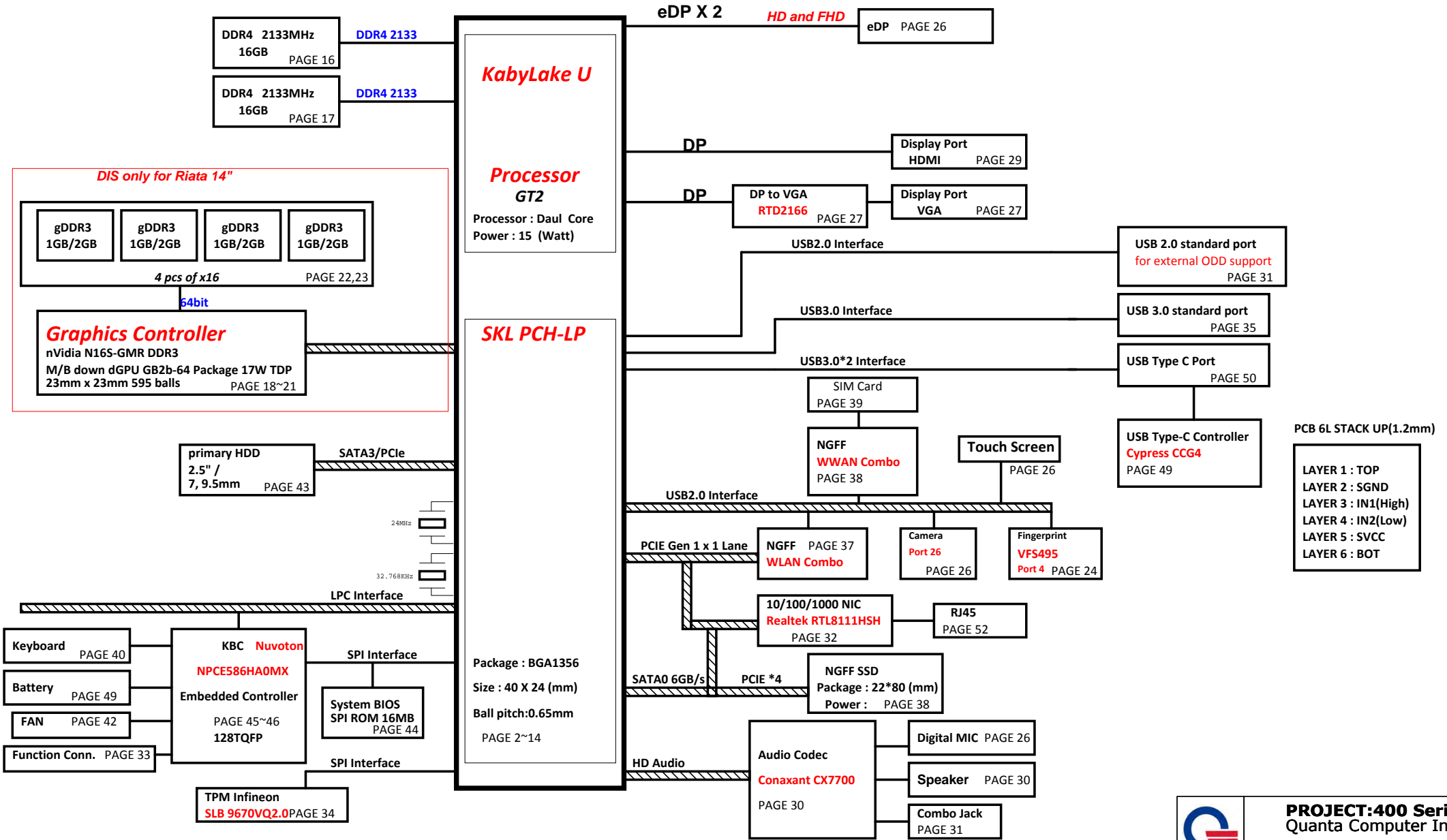
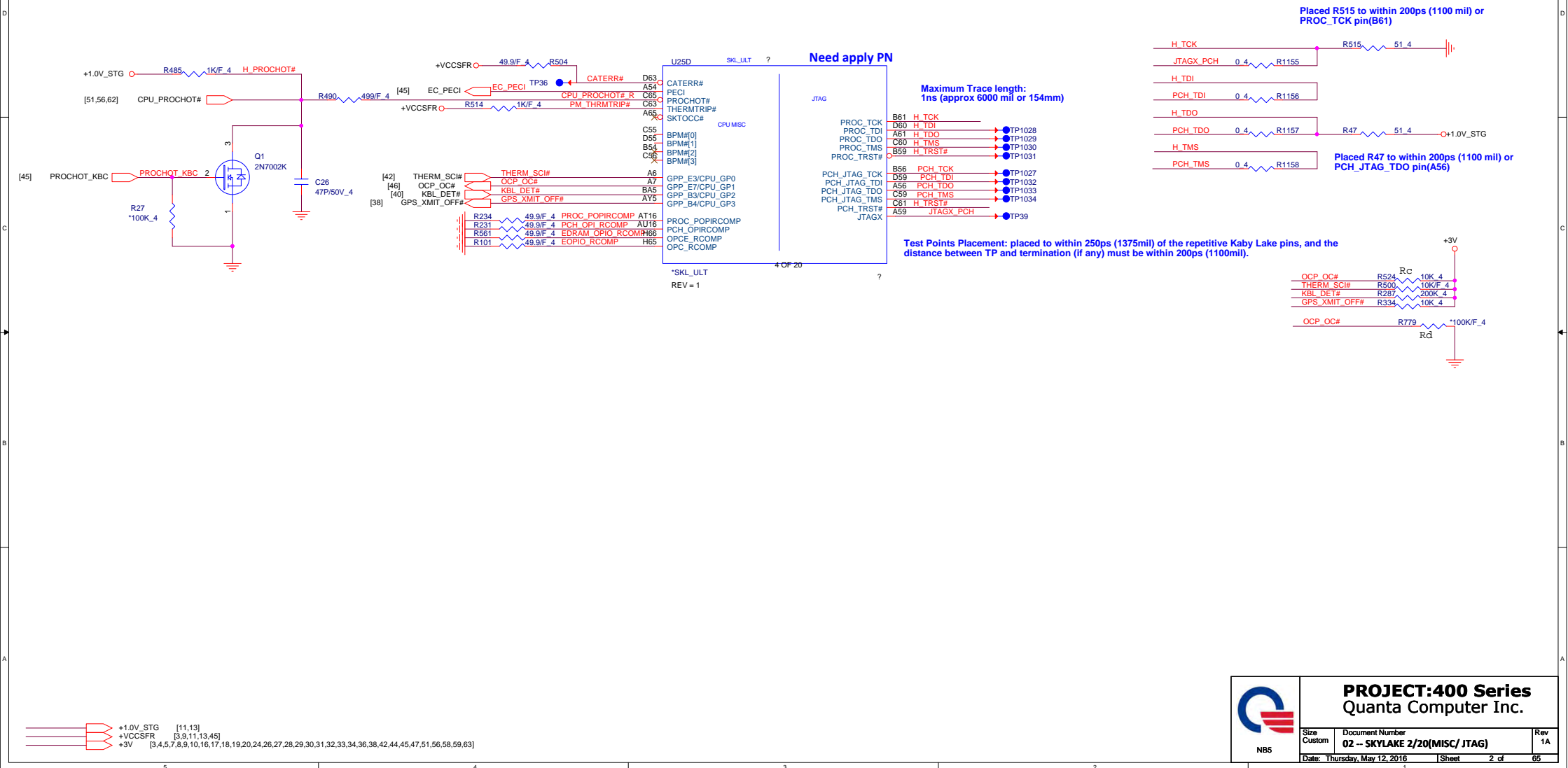
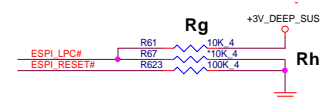
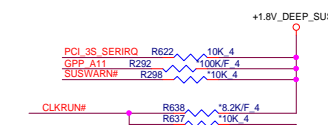
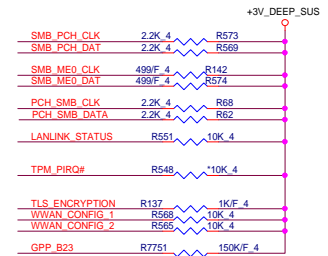
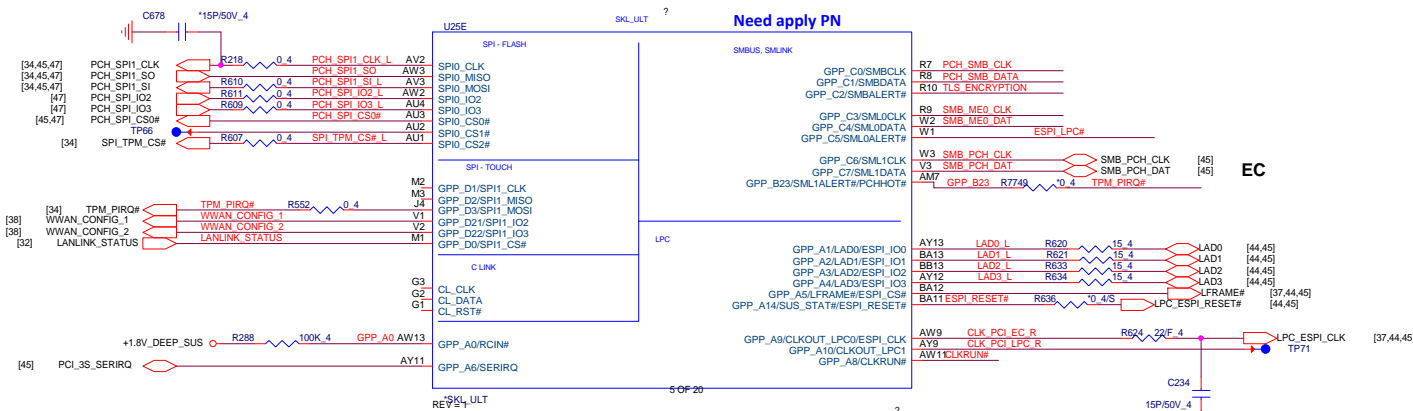


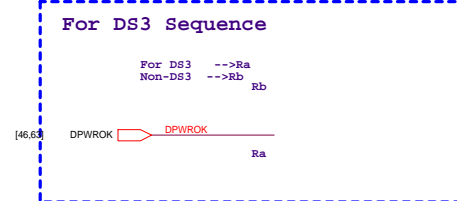
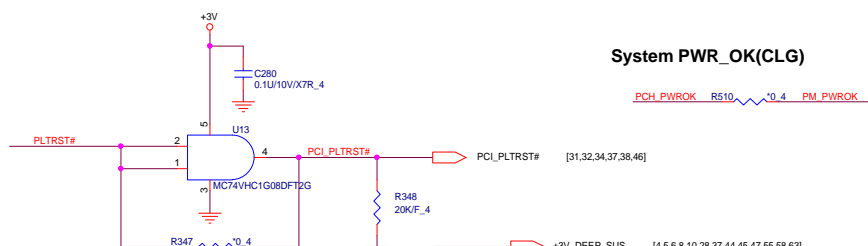
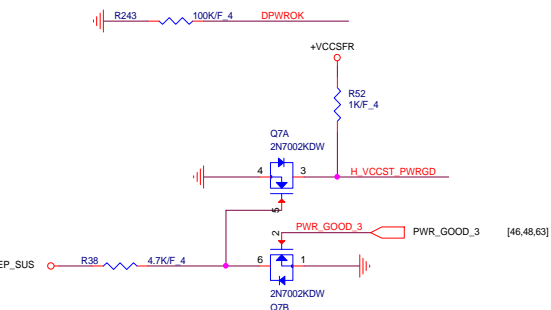
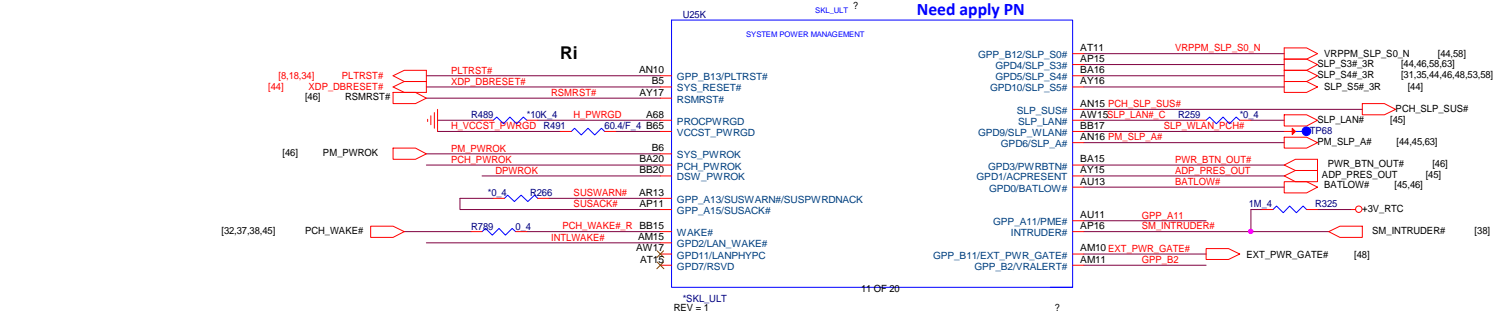
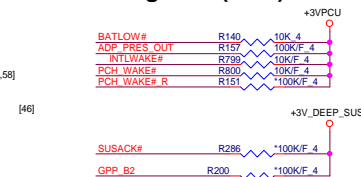
Reilly 13"/Rourke 14" KabyLake -U (UMA/DIS) Schematics01







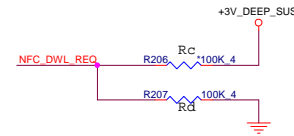
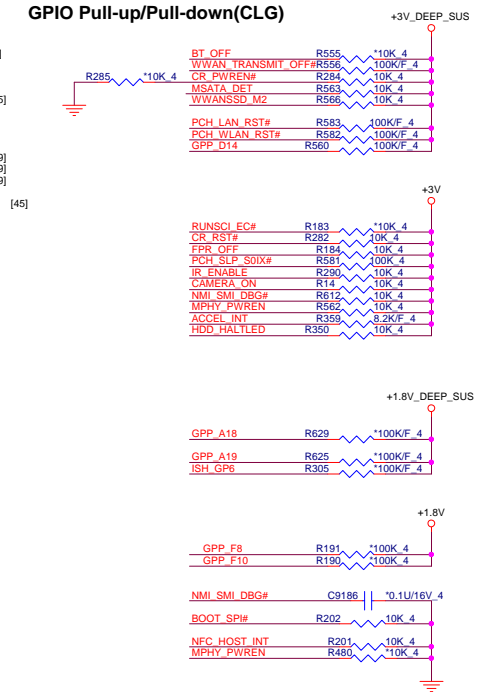
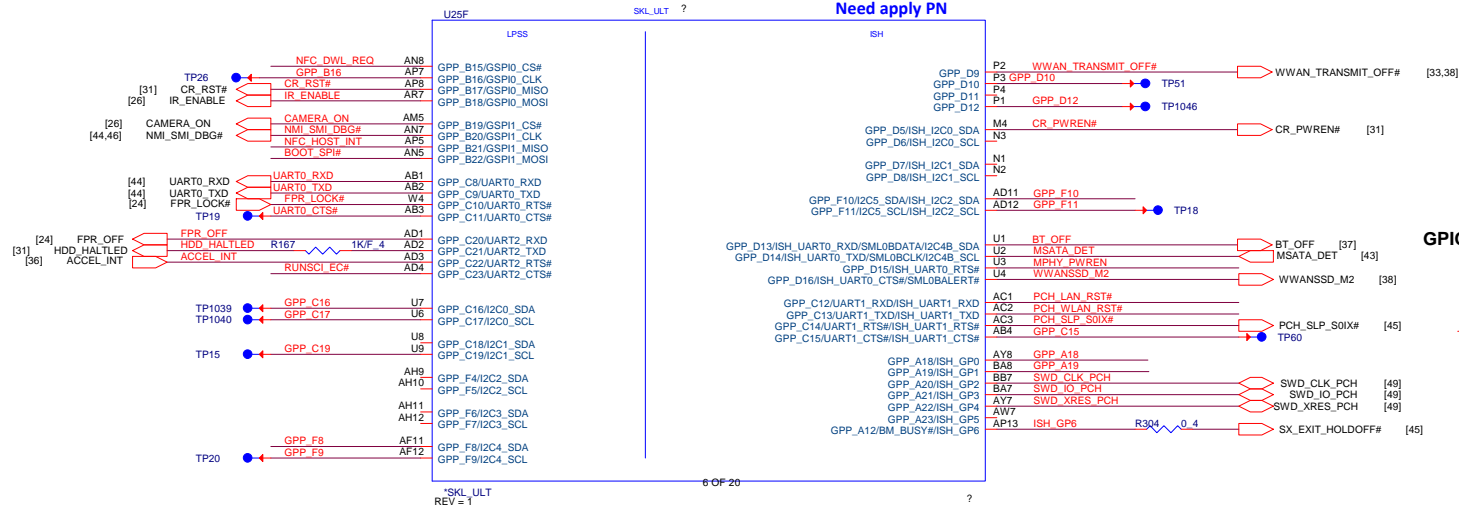
PCH Pull-high/low(CLG)



PROJECT:400 Series
Quanta Computer Inc.

Size Custom
Document Number
03 -- SKYLAKE (SPI/LPC/SMB/PM)
Rev 1A

Date: Thursday, May 12, 2016
Sheet 3 of 65



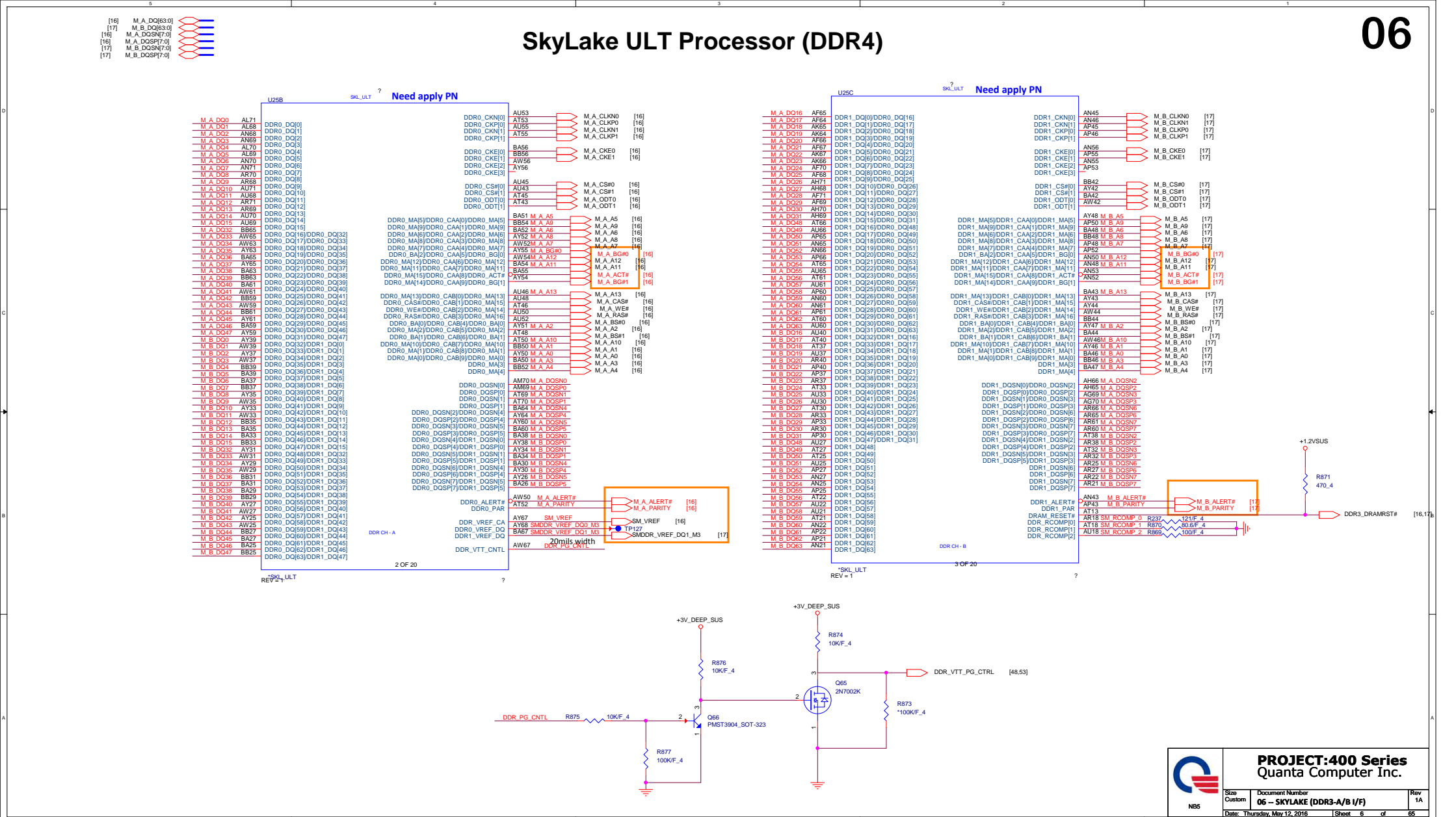
Codec table		
	CX7700	CX7501
R206	INSTAL	UNINSTAL
R207	UNINSTAL	INSTAL

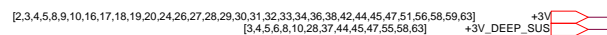
[2,3,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]

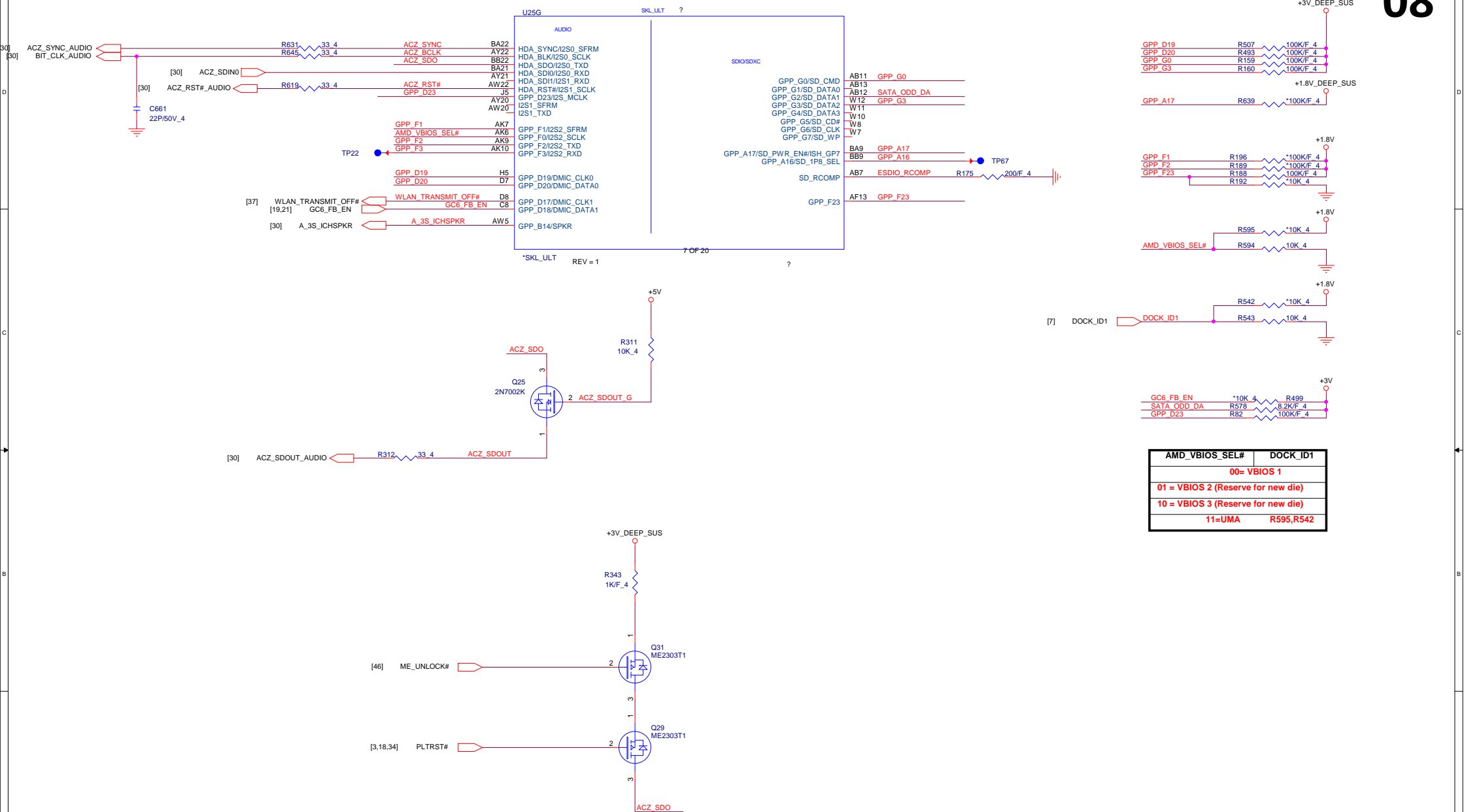


PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 04 -- SKYLAKE (GPIO)	Rev 1A
Date: Thursday, May 12, 2016	Sheet	4 of 65



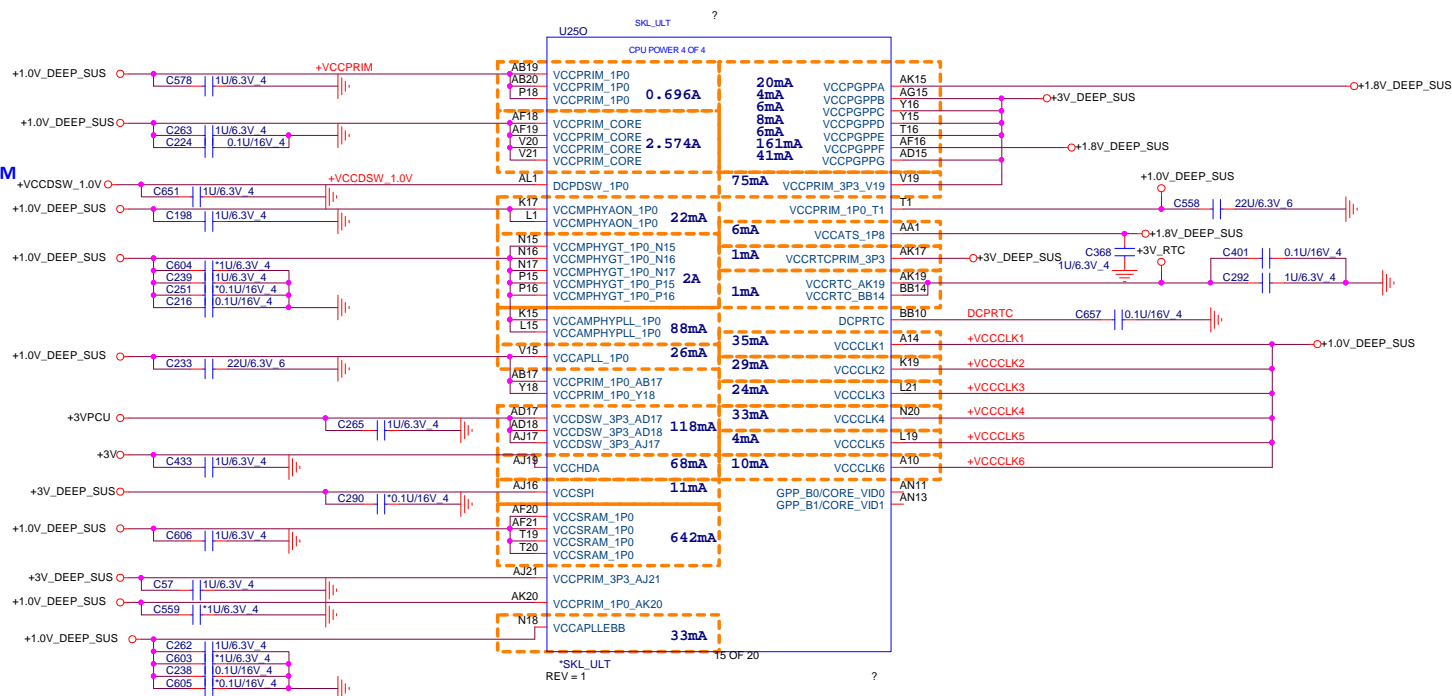





D

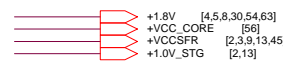
[illegible][illegible]


PCH Internal VRM

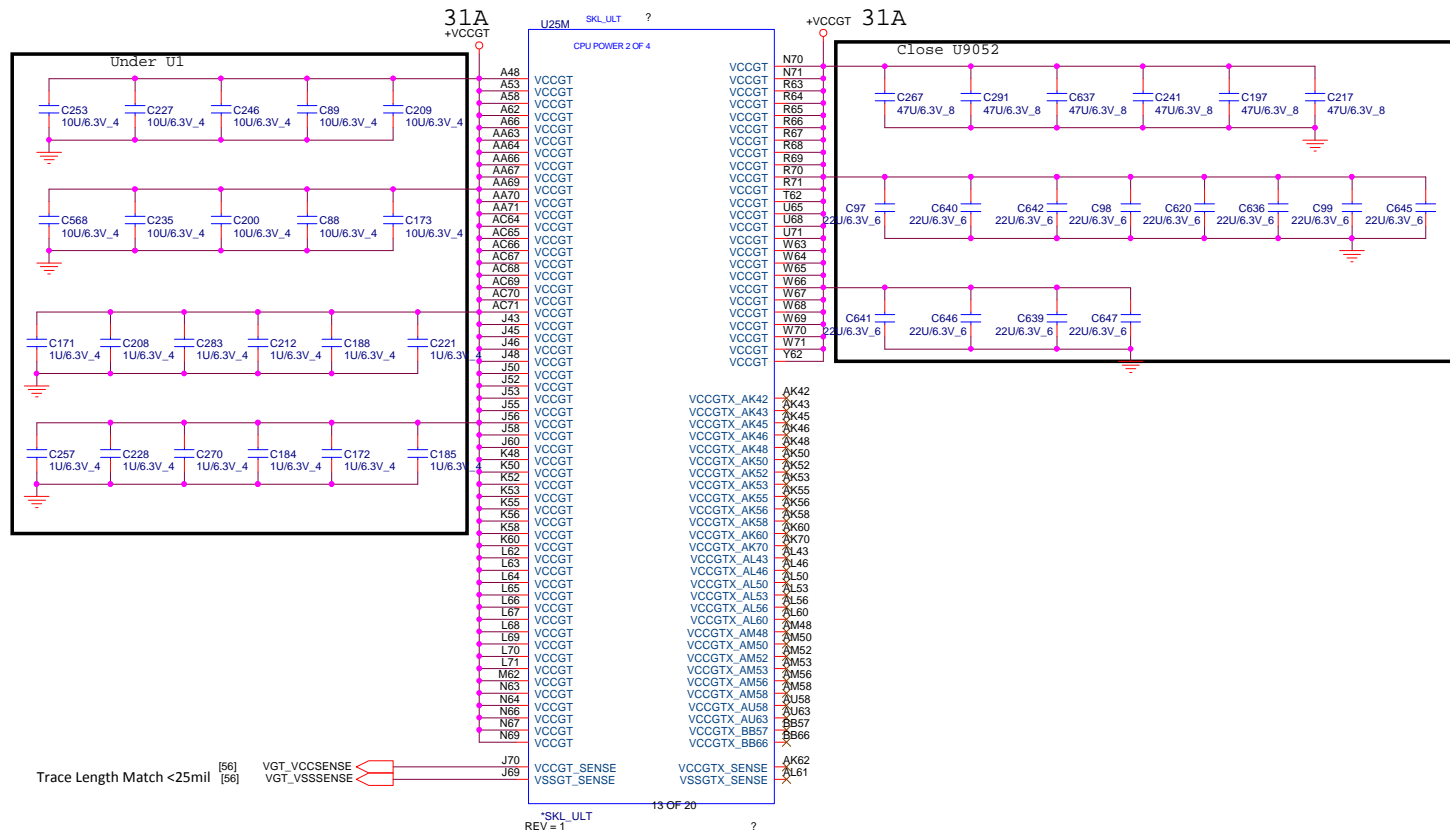


+3V_DEEP_SUS	[3,4,5,6,8,28,37,44,45,47,55,58,63]
+3VPCU	[3,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63]
+1.0V_DEEP_SUS	[9,54,55,58]
+VCC_PRIM	
+3V	[2,3,4,5,7,8,9,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]
+1.8V_DEEP_SUS	[3,4,7,8,9,45,54,63]


 PROJECT:400 Series Quanta Computer Inc.		
Size Custom	Document Number 10 - SKYLAKE (PCH POWER)	Rev 1A
Date: Thursday, May 12, 2016	Sheet 10 of 65	



 NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 11 -- SKYLAKE (POWER-1)	Rev 1A
	Date: Thursday, May 12, 2016	Sheet	11 of 65

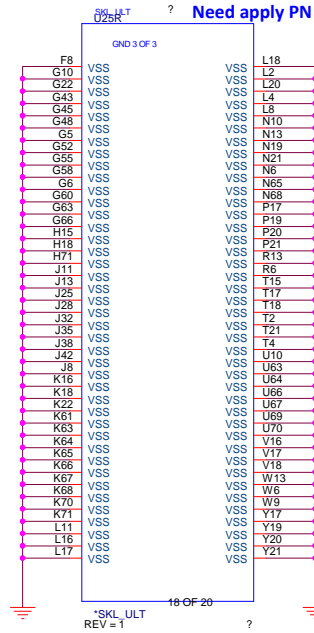
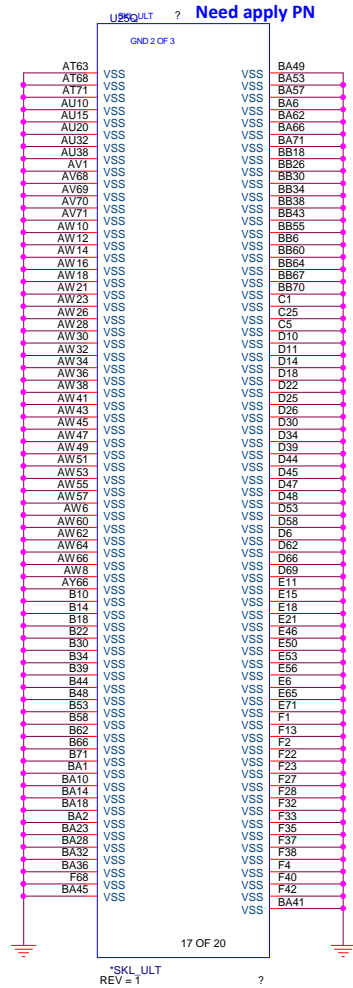
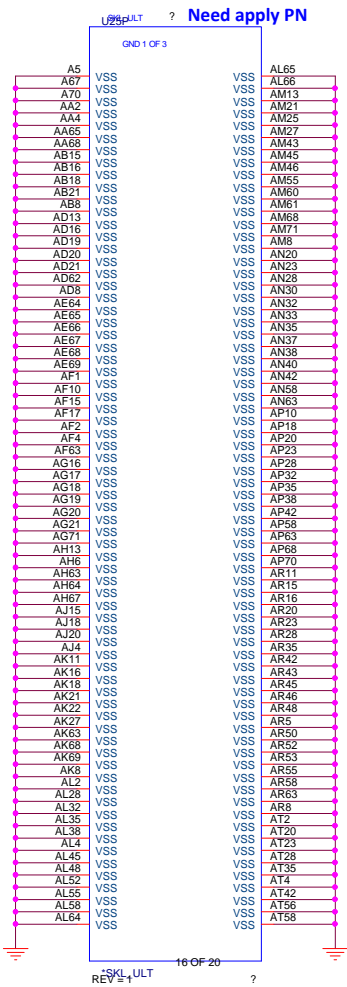



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

 NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 12 - SKYLAKE (POWER-2)	Rev 1A
	Date: Thursday, May 12, 2016	Sheet 12 of 65	

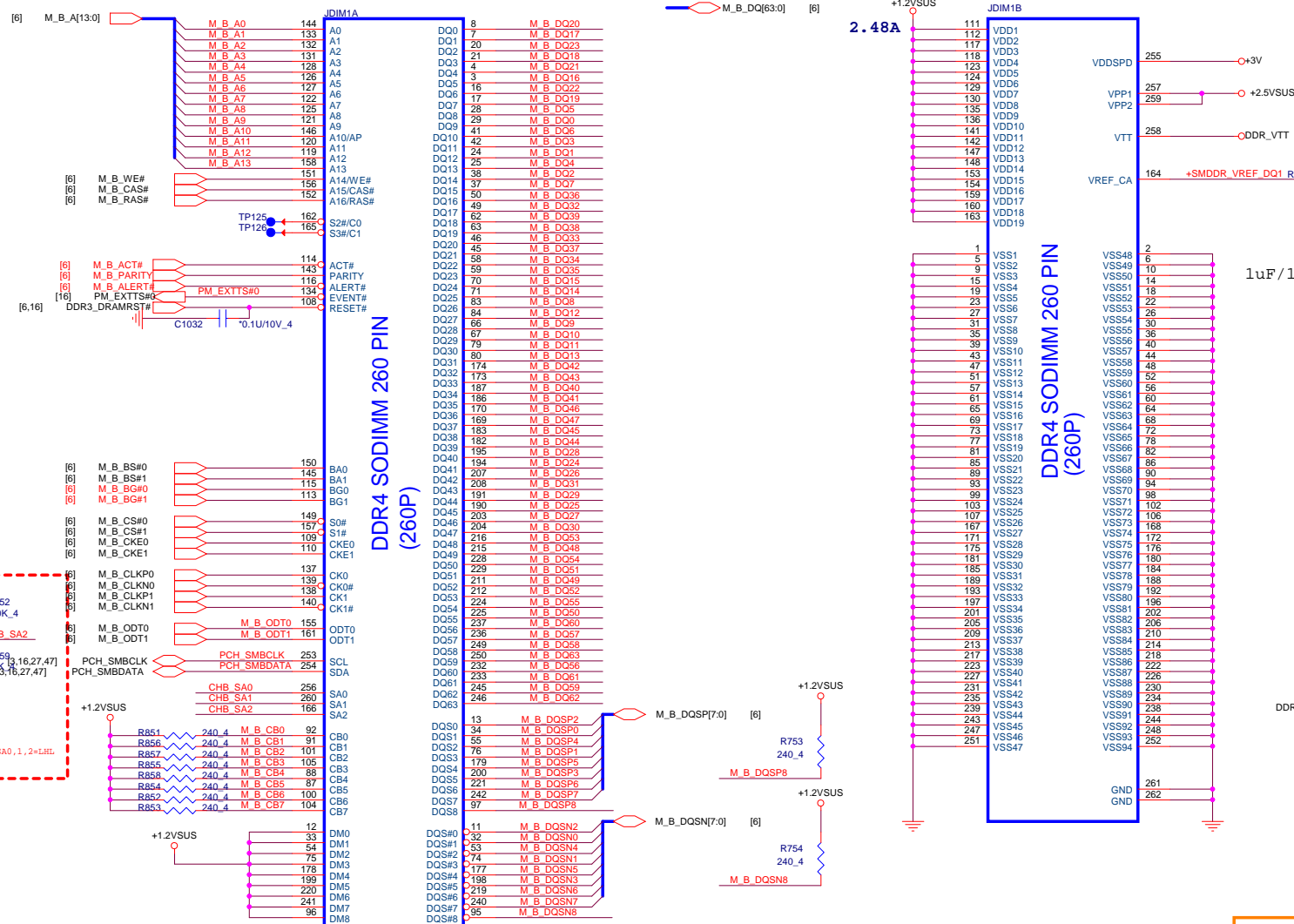


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



 NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size	Document Number	Rev
	15 -- HSW XDP & APS		1A
Date: Thursday, May 12, 2016		Sheet	15 of 65

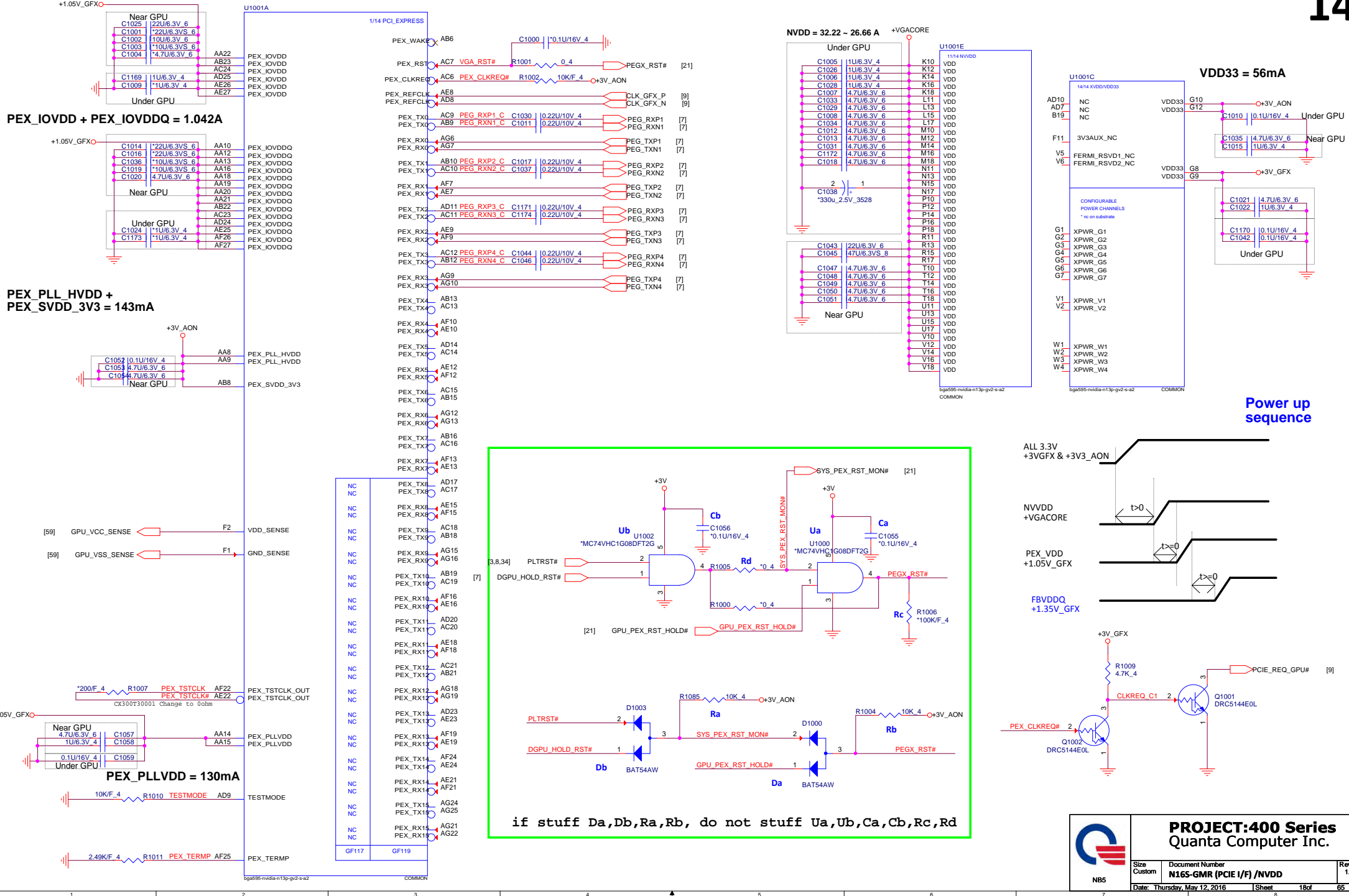


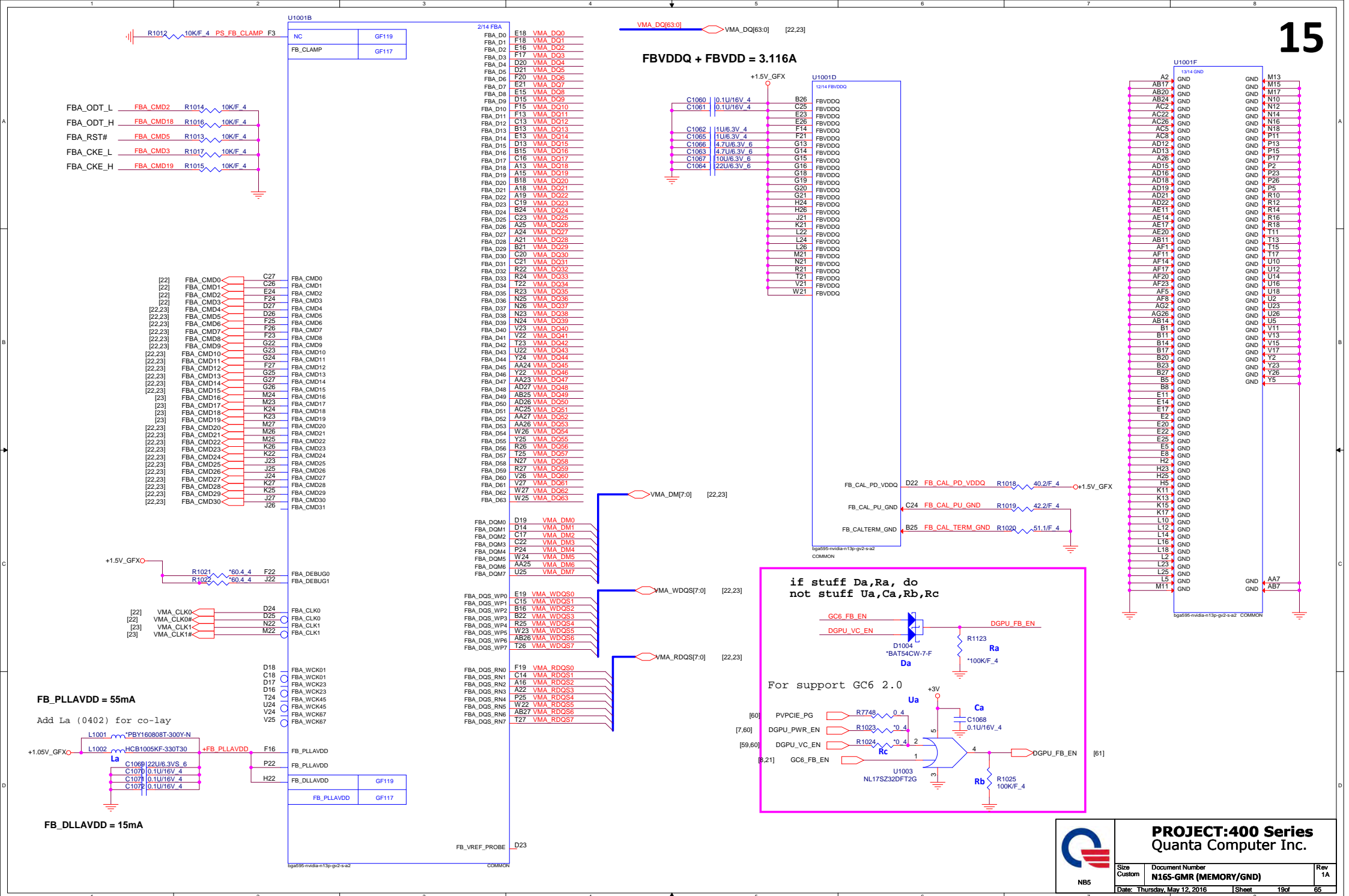


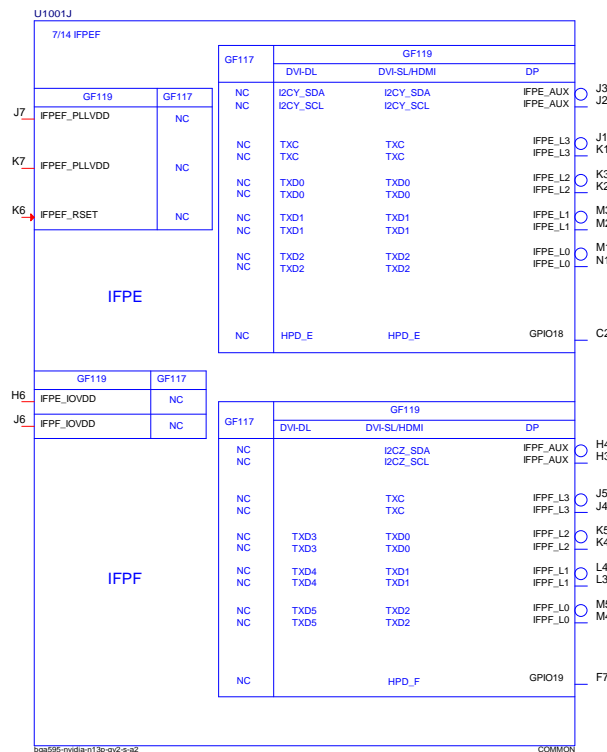
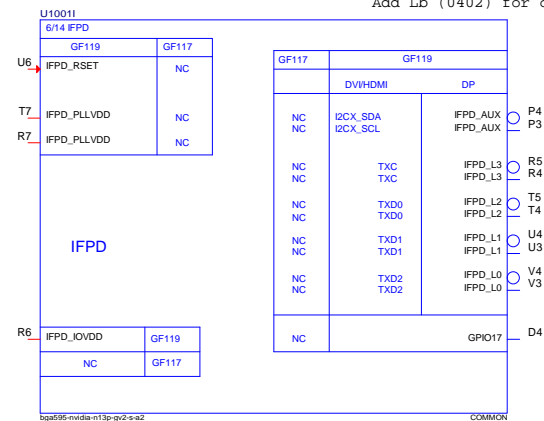
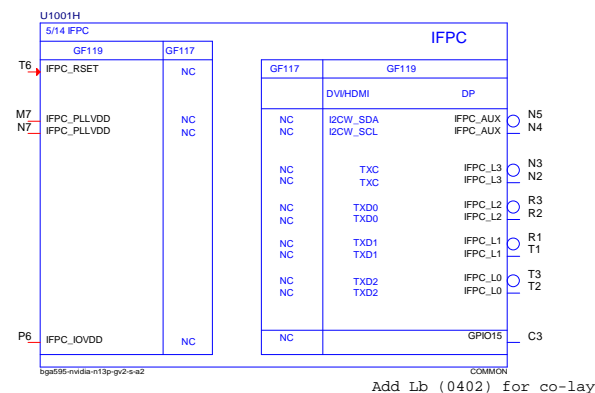
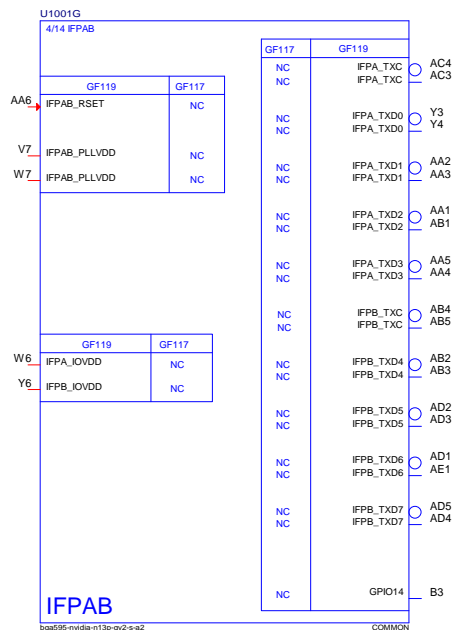
PEX_IOVDD + PEX_IOVDDQ = 1.042A

PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA

PEX_PLLVDD = 130mA



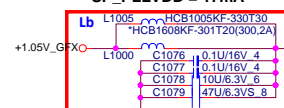




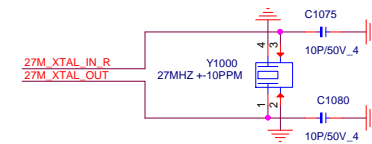
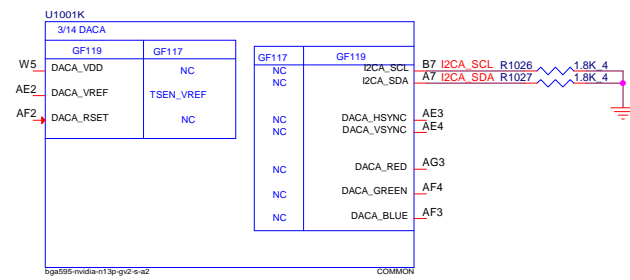
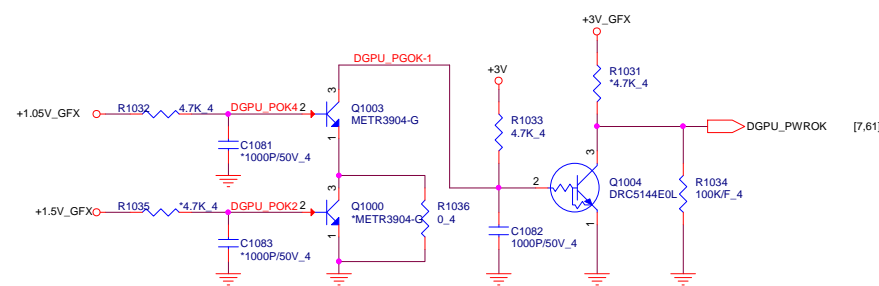
PLLVDD = 38mA Add Ia (0402) for co-layer

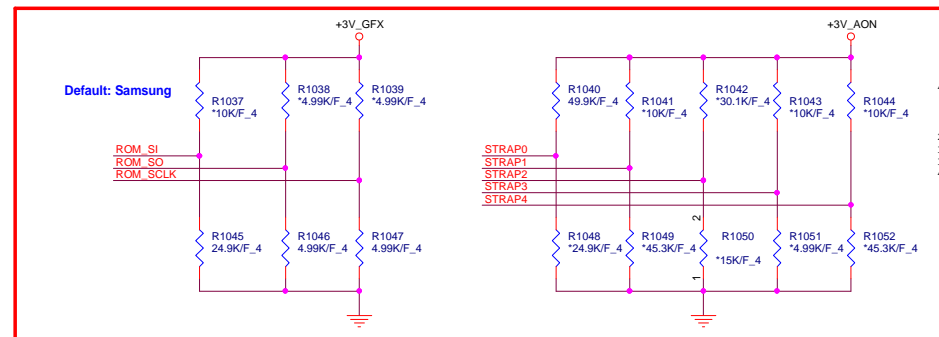
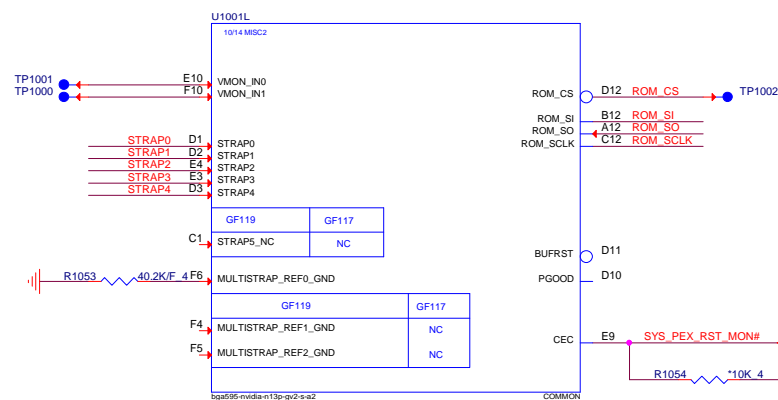


SP_PLLVDD = 17mA



VID_PLLVDD = 41mA

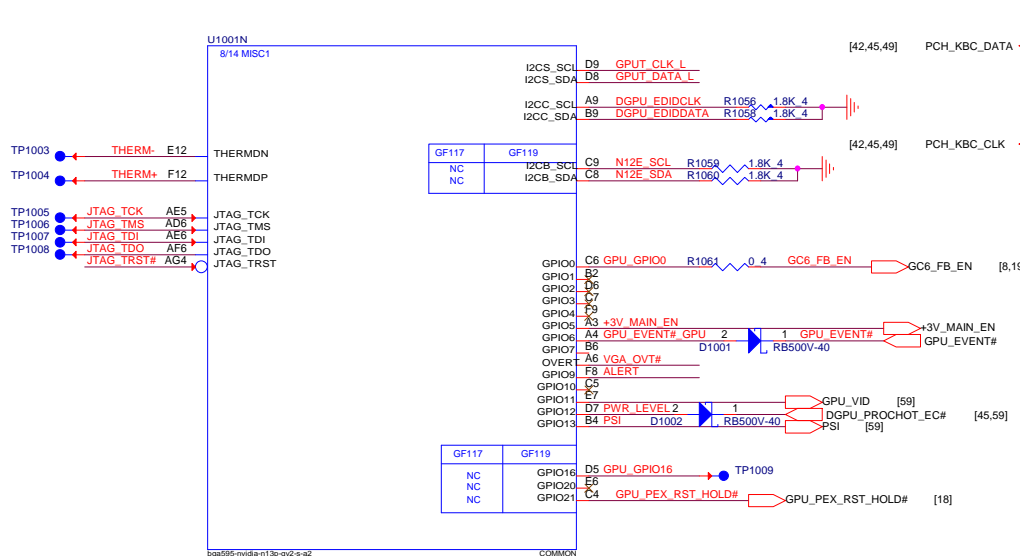




4.99k	CS24992PB26
10k	CS31002PB26
15k	CS31502PB24
20k	CS32002PB29
24.9k	CS2492PB16
30.1k	CS33012PB18
34.8k	CS33482PB06
45.3k	CS34532PB18

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

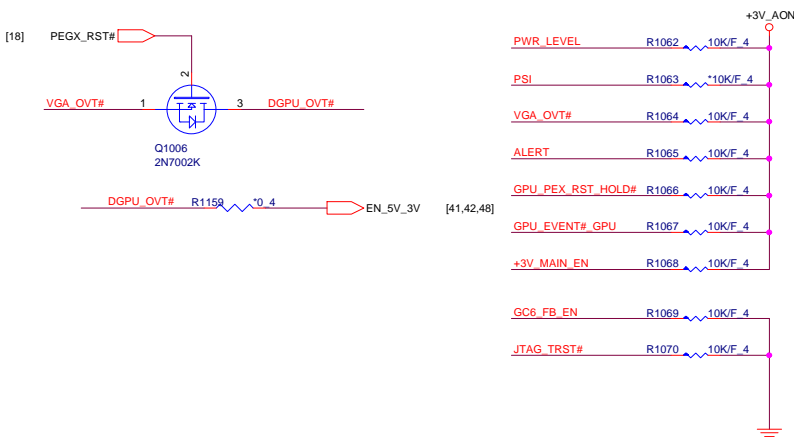


VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0000	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
0101	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 - 256Mx16, 1.5V, 1Ghz/1.35V 900Mhz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY_VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



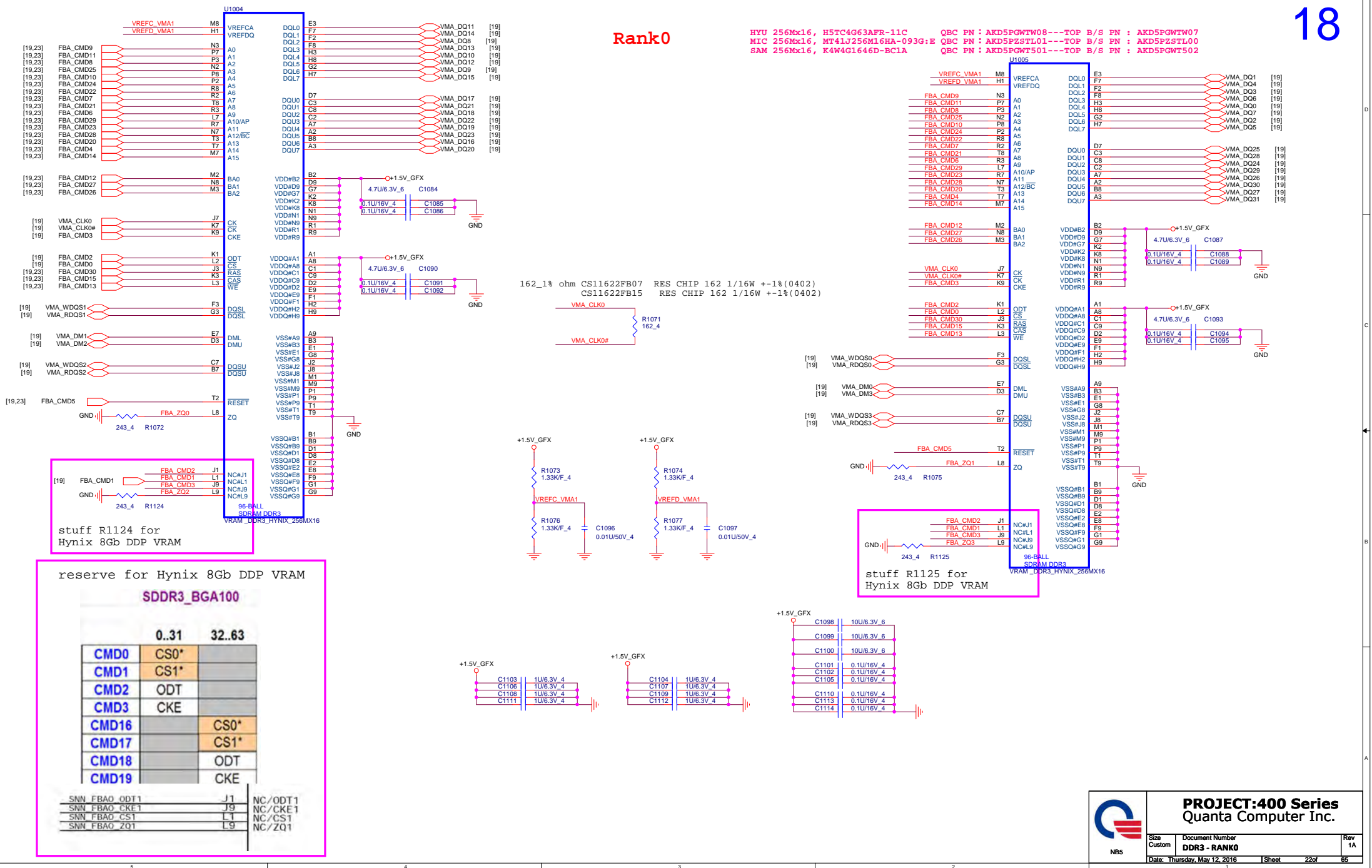
PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16S-GMR (GPIO/STRAPS)	1A
Date: Thursday, May 12, 2016	Sheet 21 of 65	

Rank0

HYU 256Mx16, H5TC4G63APR-11C
MTC 256Mx16, MT41J256M16BA-093G:E
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



PROJECT:400 Series
Quanta Computer Inc.

Size Custom

Document Number
DDR3 - RANK0

Rev 1A

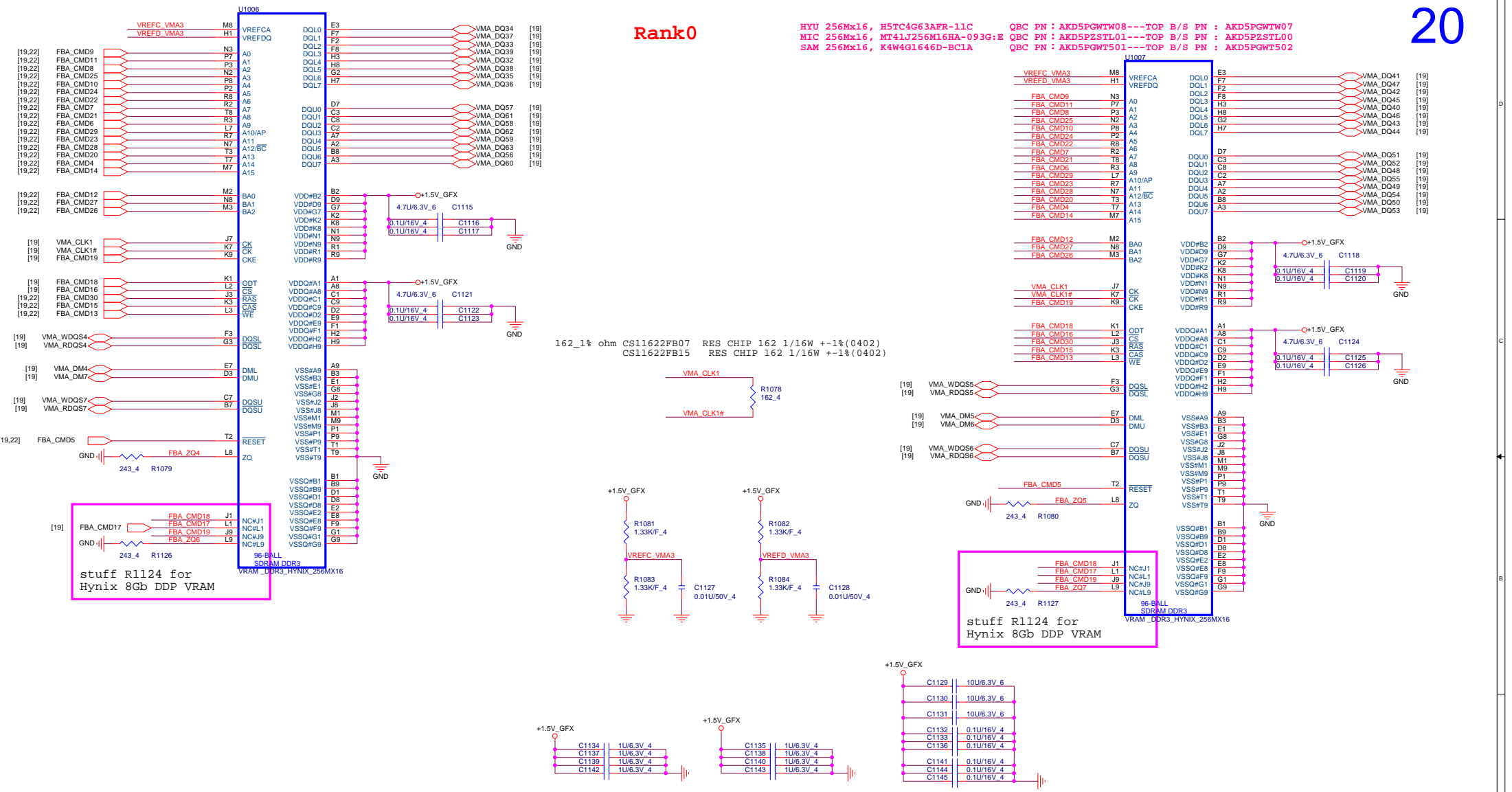
Date: Thursday, May 12, 2016

Sheet 22 of 85

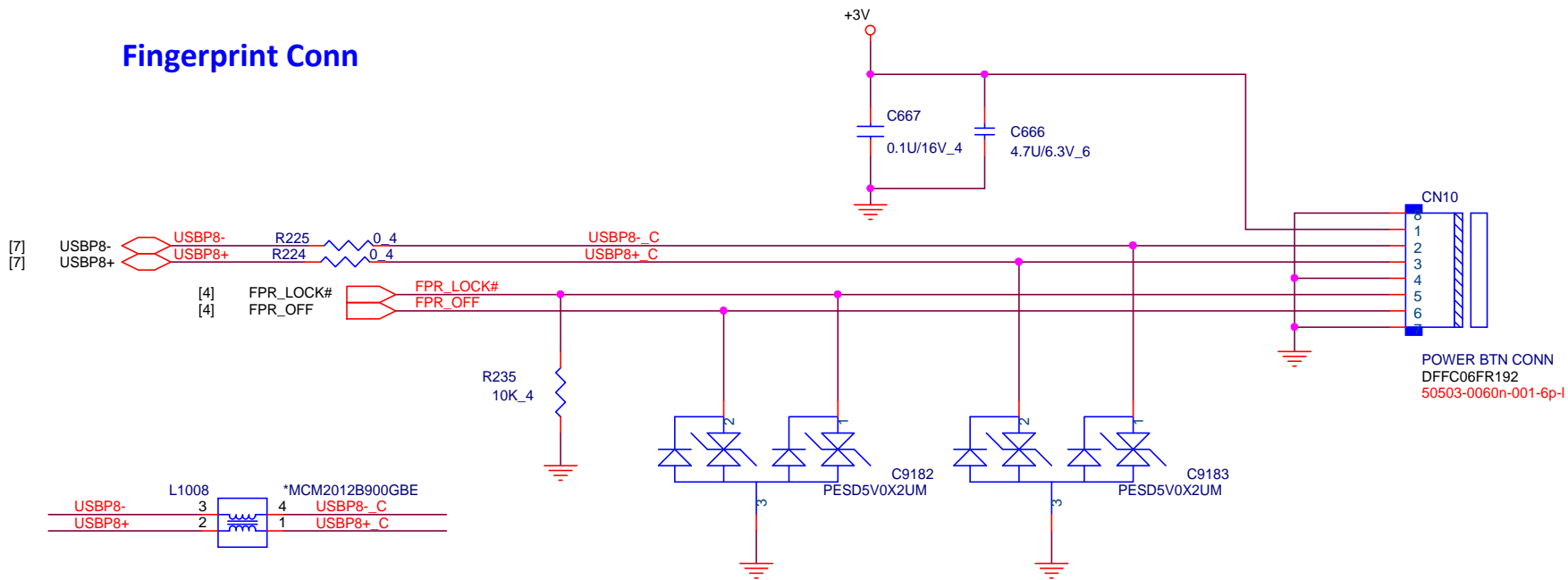
Rank0

HYU 256Mx16, H5TC4G63AFR-11C
MIC 256Mx16, MT41J256M16HA-093G:E
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



Fingerprint Conn



PROJECT:400 Series
Quanta Computer Inc.

Size	Custom
------	--------

Document Number

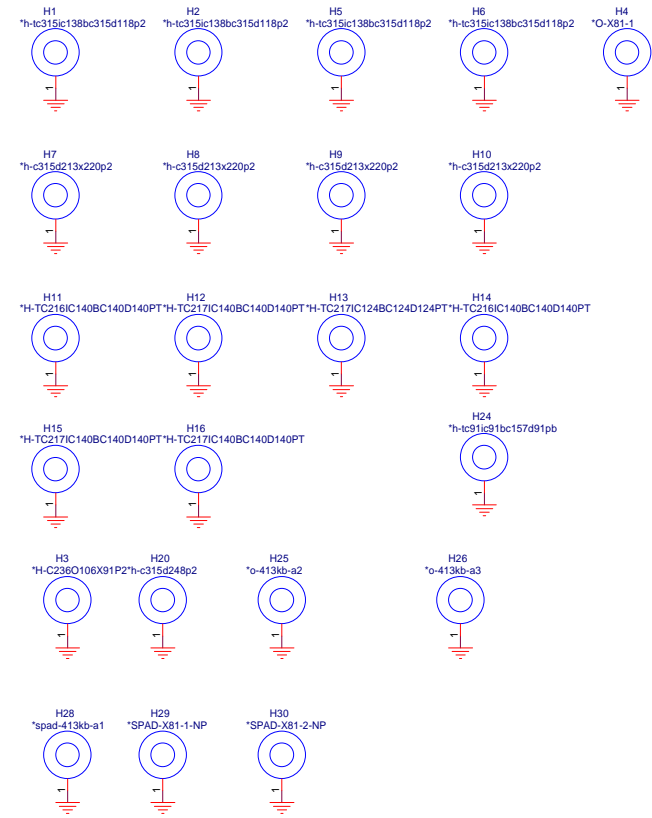
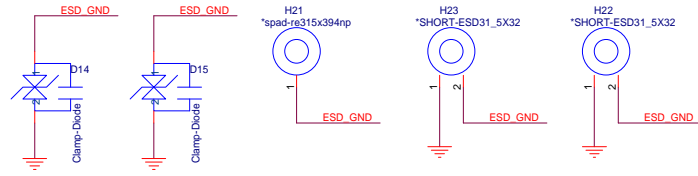
24 -- FPR

Rev
1A

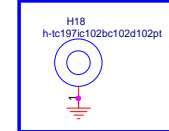
Date: Thursday, May 12, 2016

Sheet 24 of 65

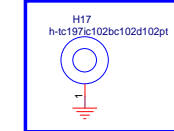
Hole



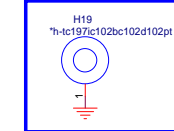
WLAN nut



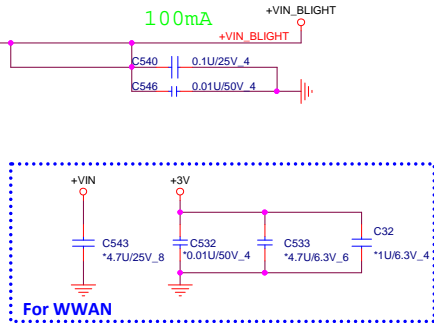
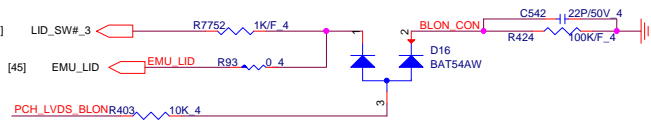
SSD nut



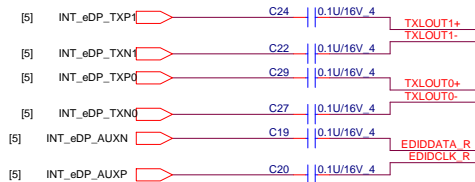
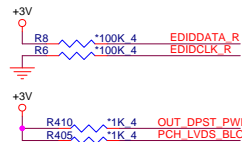
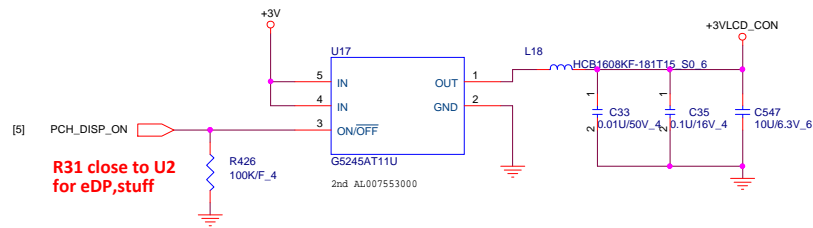
WWAN nut



LID Switch



For eDP
Close to LVDS connector



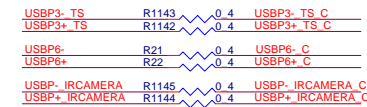
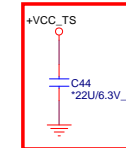
ALF@20151019:

1. Designed Reserve 4Pins for IR CCD Pin 26 to Pin29
2. Combined the +3V & +3V_CAM & +3V_IR at Pin26~25

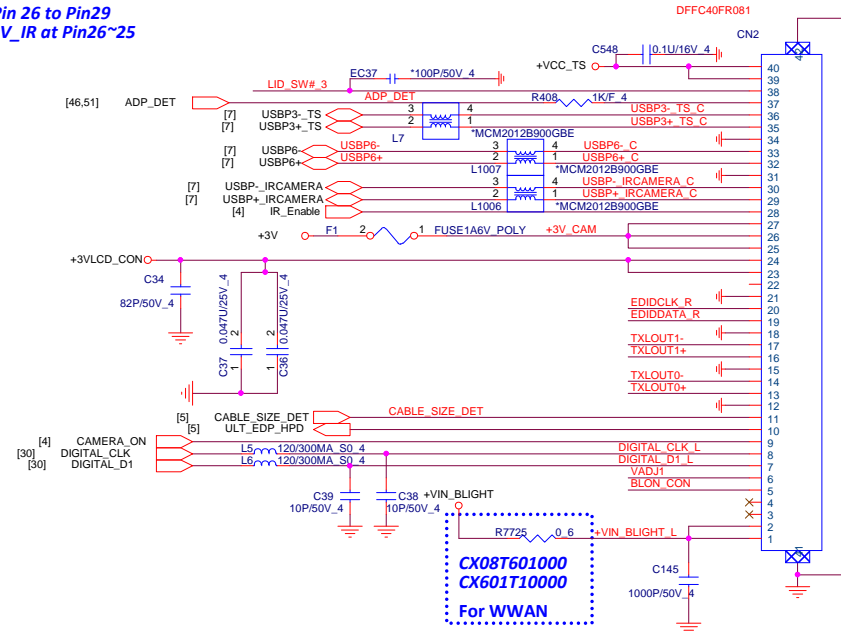


LVDS Conn.

26



GS12401-1011-9H
lvds-50671-04041-001-40p-I



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]
[8,27,29,30,40,42,43,54,58,63]
[28,44,51,52,53,54,55,56,57,58,59,61,66]

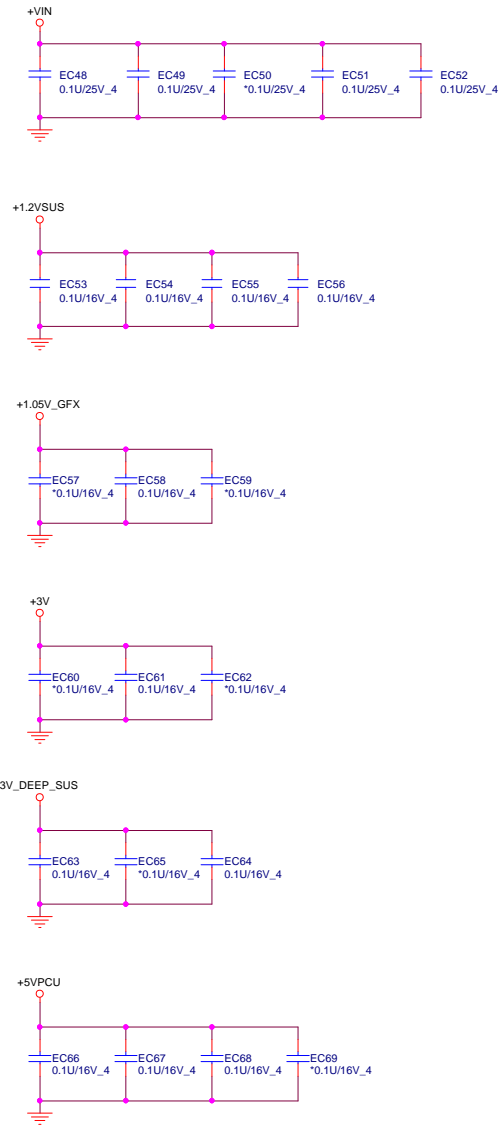
+3V
+5V
+VIN



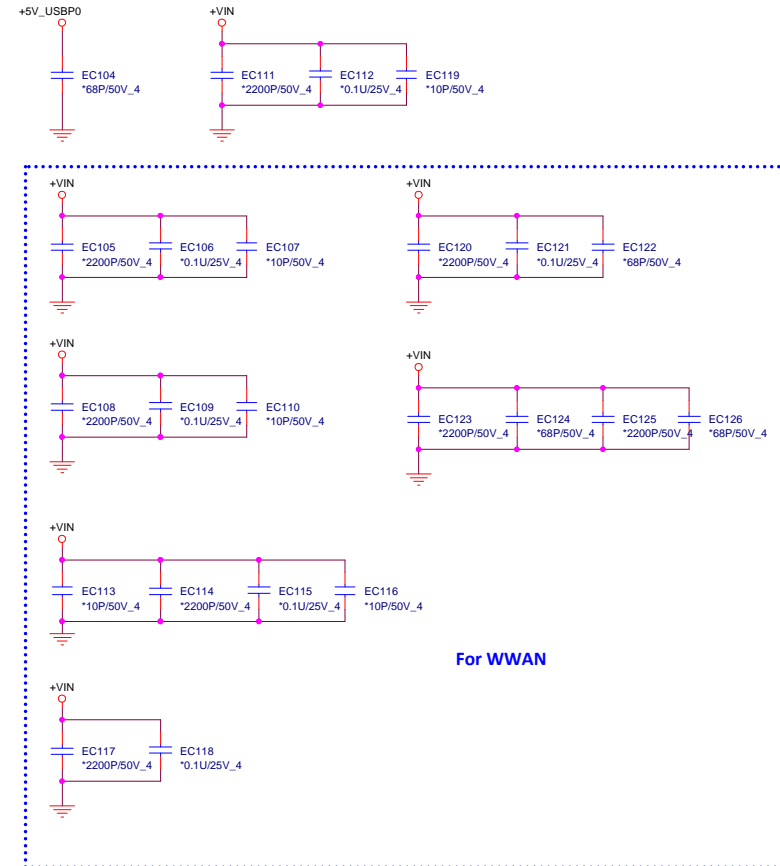
PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 26 - LCD CONN/LID/CAM/D-MIC	Rev 1A
Date: Thursday, May 12, 2016	Sheet 26 of 65	

EMI CAP



RF Cap

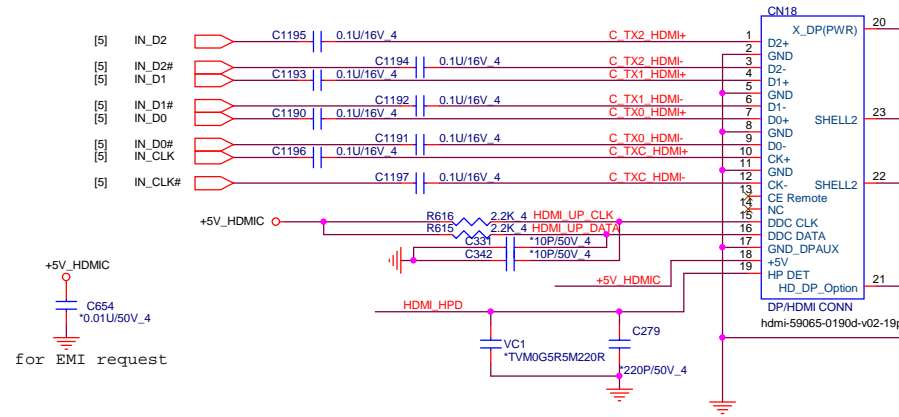
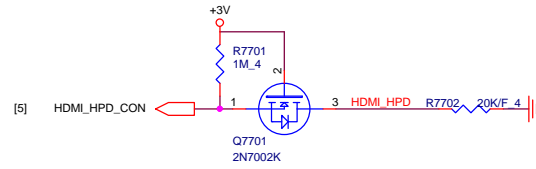


PROJECT:400 Series
Quanta Computer Inc.

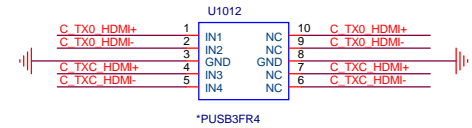
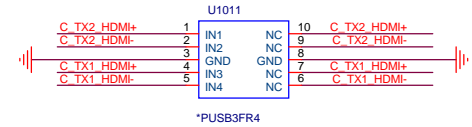
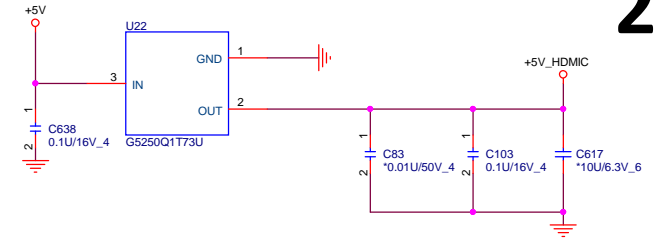
Size	Document Number	Rev
Custom	28 – REPEATER PS8407A	1A
Date: Thursday, May 12, 2016	Sheet 28 of 65	

EMI Solution

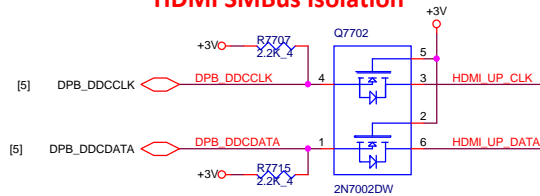
C.TX2_HDMI+	R208	120/F_4	C.TX2_HDMI-
C.TX1_HDMI+	R194	120/F_4	C.TX1_HDMI-
C.TX0_HDMI+	R178	120/F_4	C.TX0_HDMI-
C.TXC_HDMI+	R221	120/F_4	C.TXC_HDMI-



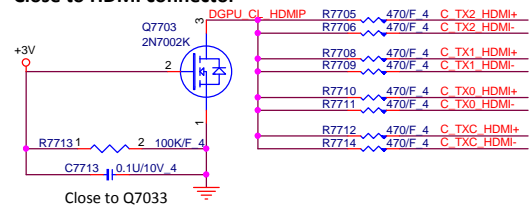
+5V_HDMIC
C654
*0.01U/50V_4
for EMI request



HDMI SMBus Isolation

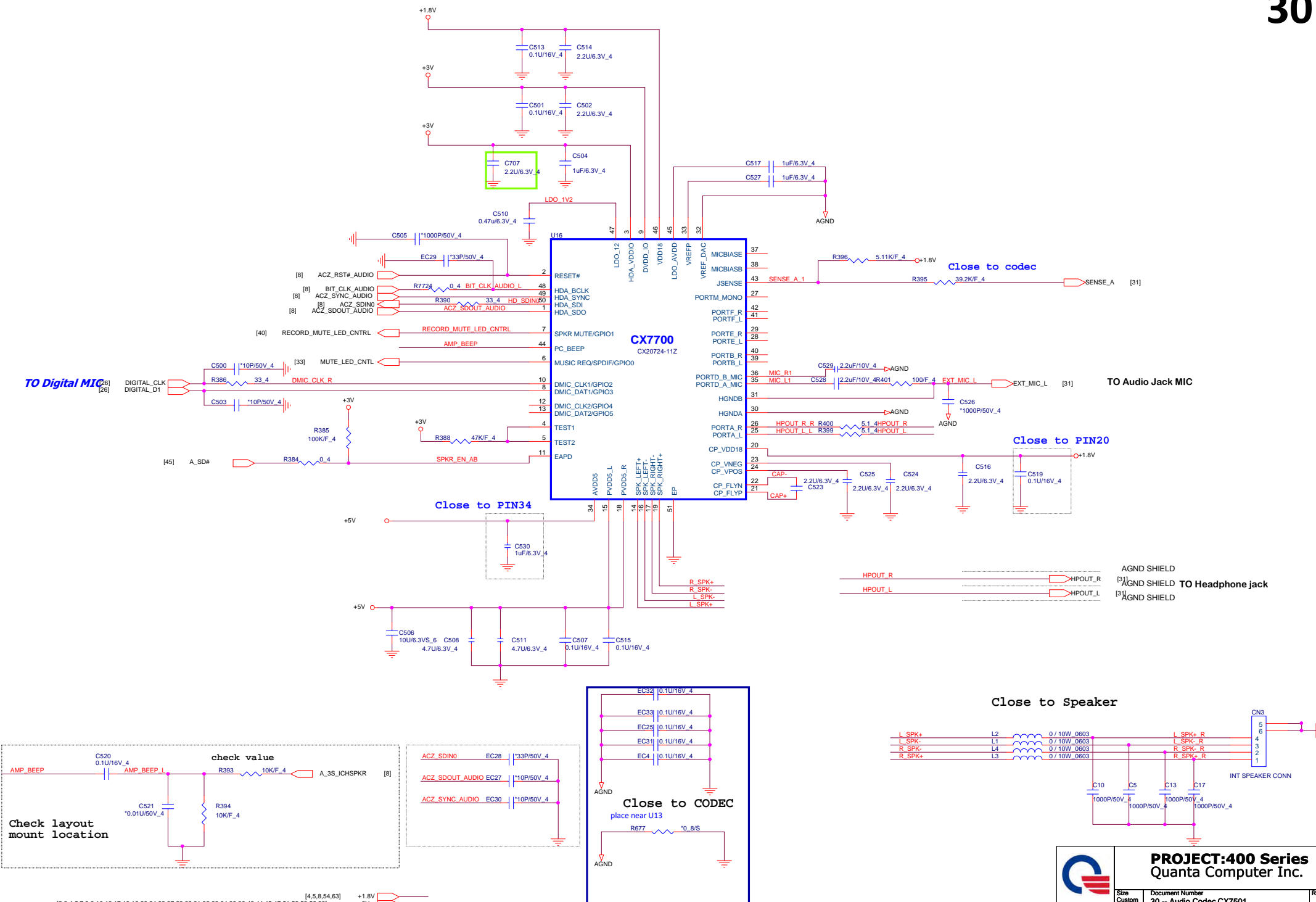


Close to HDMI connector

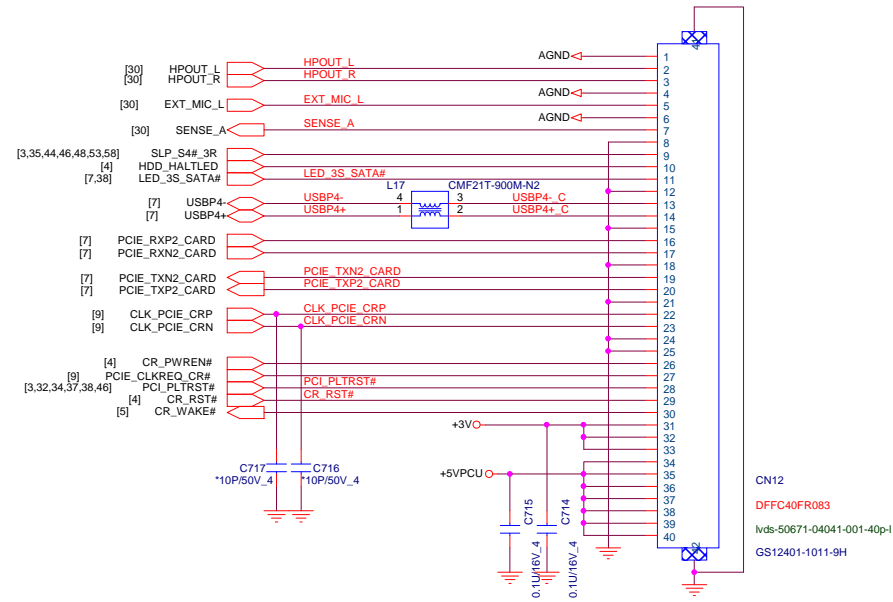


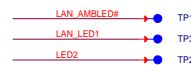
PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 29 -- HDMI CONNECTOR	Rev 1A
Date: Thursday, May 12, 2016	Sheet 29 of 65	

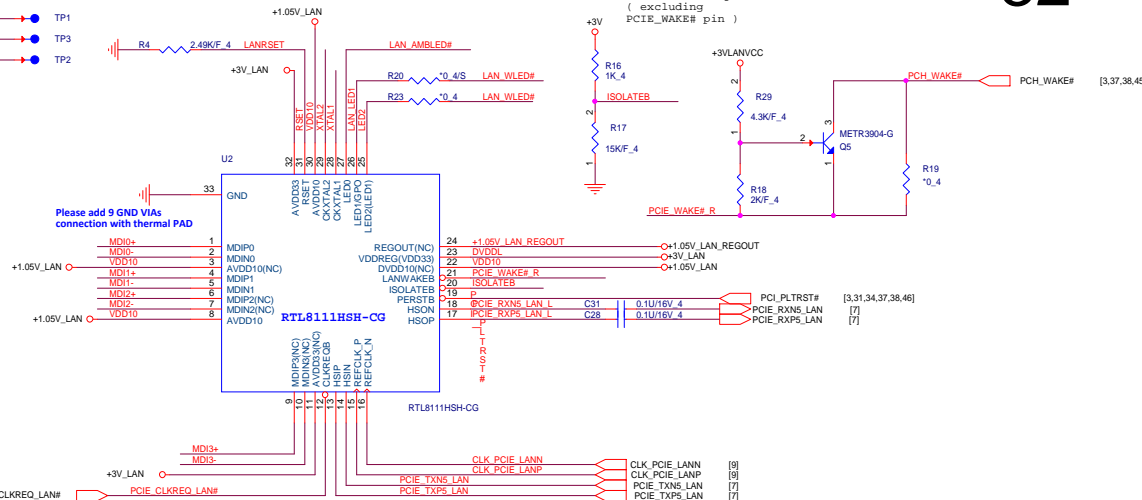


USB/Card Reader/Headphone_Mic Combo Jack Daughter Board Connector



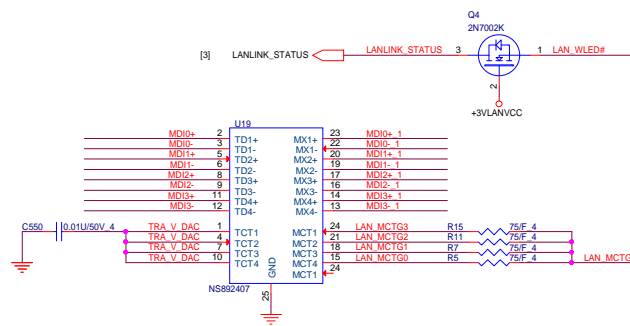
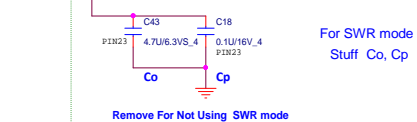
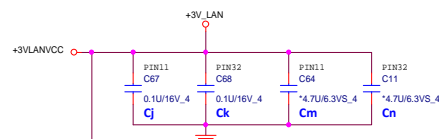


```
if ISOLATEB pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE_WAKE# pin )
```

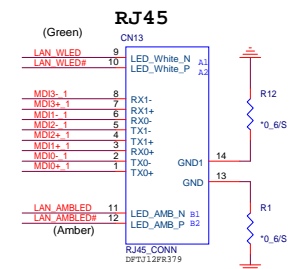


The schematic shows two input lines, +3V/LANVCC, connected to two LEDs. The top LED is labeled LAN_WLED and the bottom LED is labeled LAN_AMBLD. Each LED is connected to ground through a resistor (R3 and R28, both 330Ω) and a capacitor (C7 and C56, both 1000pF/50V).

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

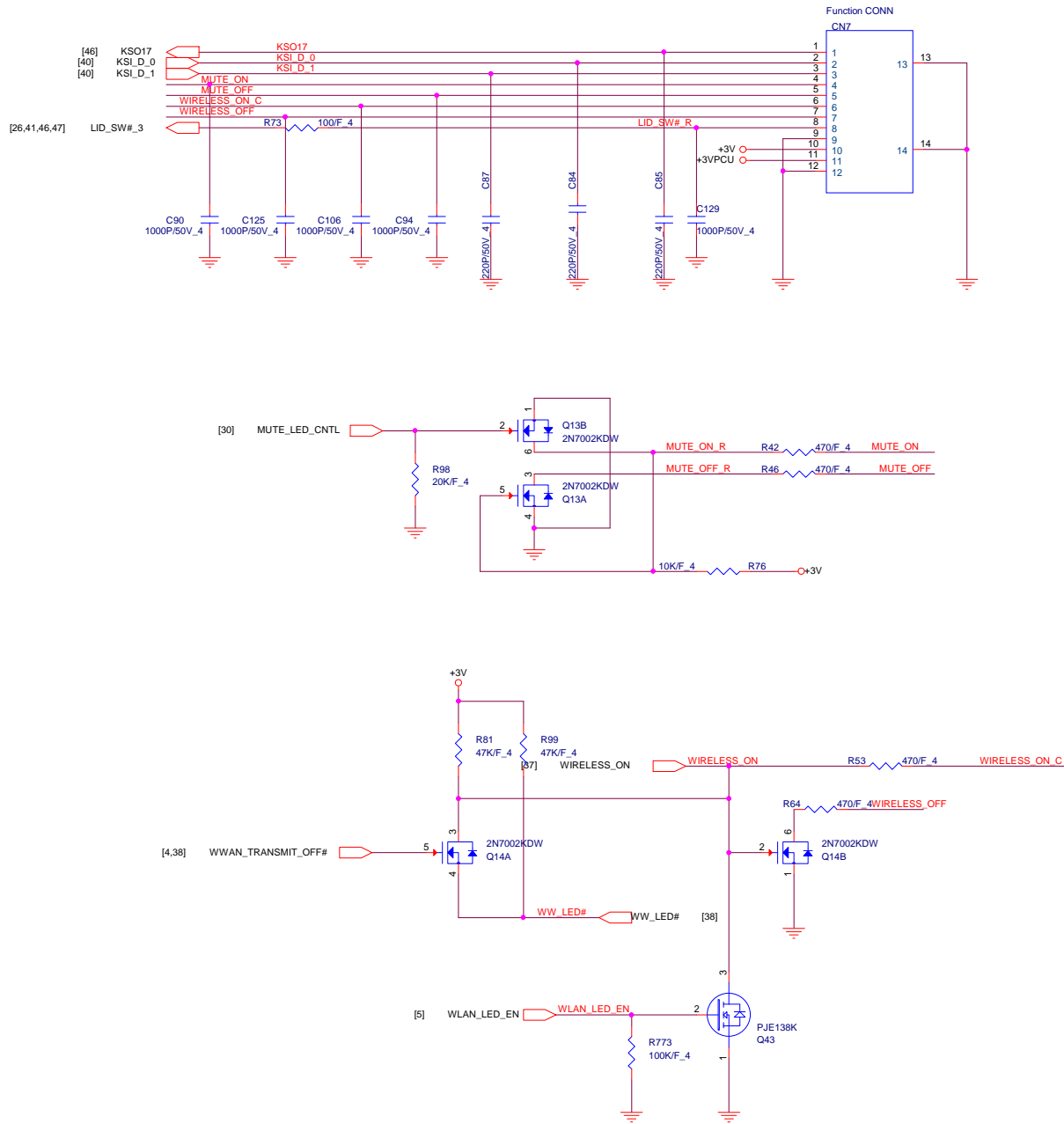


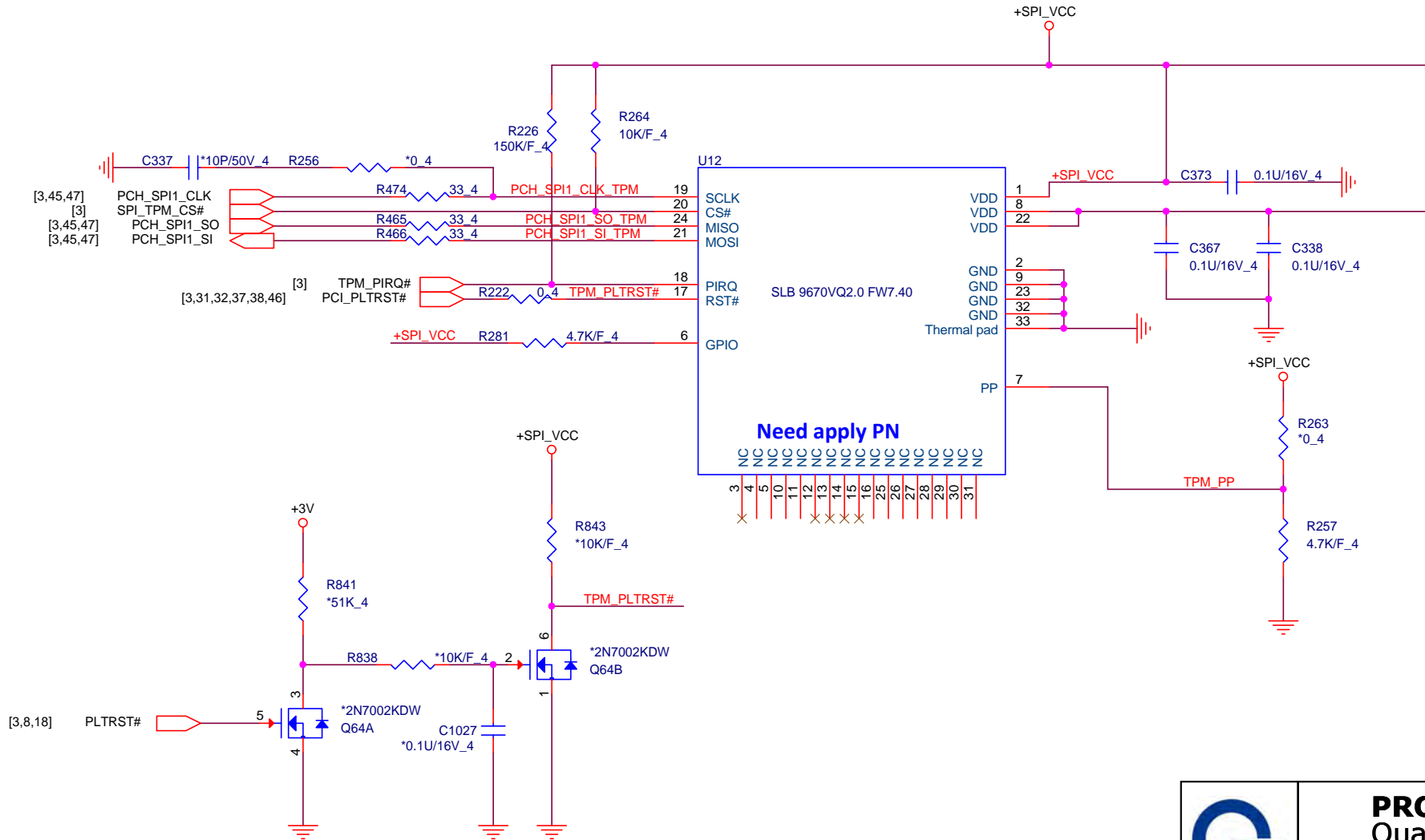
For GiGA BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00




[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,33,34,36,38,42,44,45,47,51,56,58,59,63]

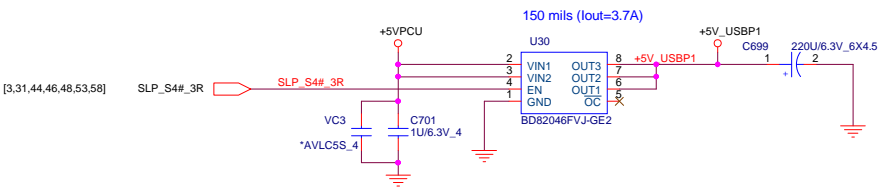
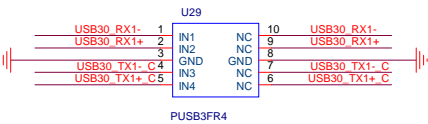
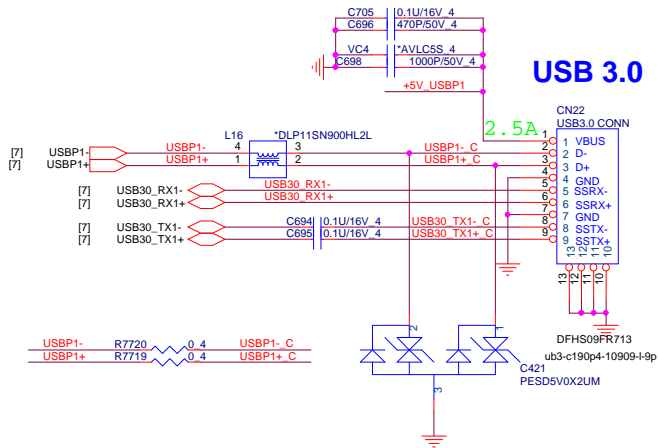
[58] +3V
+3VLANVCC





 PROJECT:400 Series Quanta Computer Inc.		
Size Custom	Document Number 34 -- TPM SLB9670_QFN	Rev 1A
Date: Thursday, May 12, 2016		Sheet 34 of 65

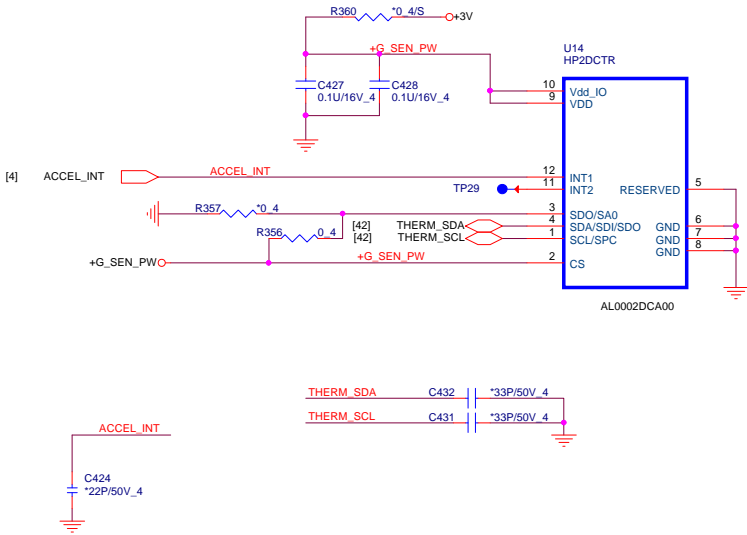
USB 2.0/3.0 Combo



[28,31,44,49,50,51,52,53,54,56,57,58,59,60,61,63] +5VPCU


[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63] +3VPCU

Accelerometer Sensor



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,38,42,44,45,47,51,56,58,59,63] +3V

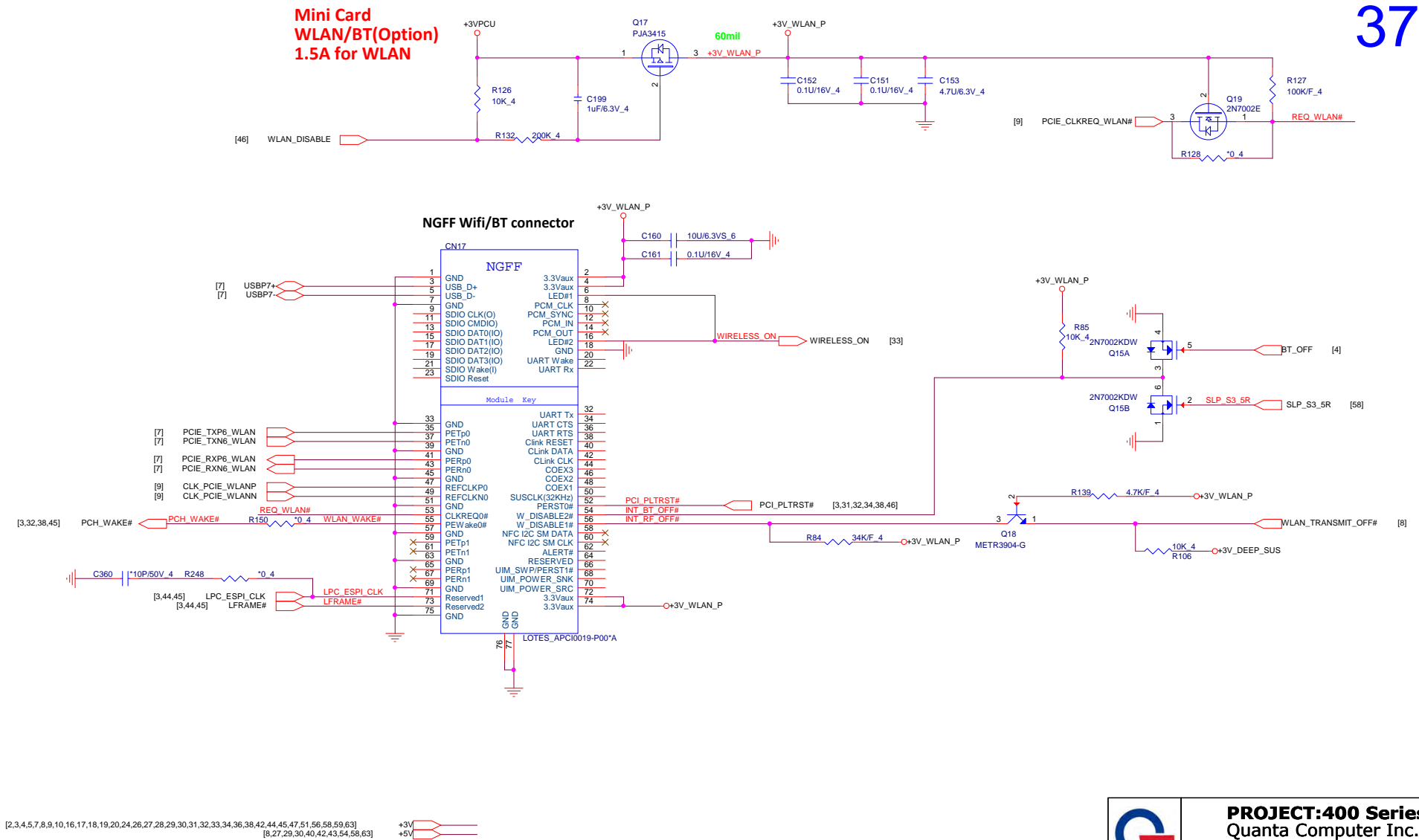
[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63] +3VPCU

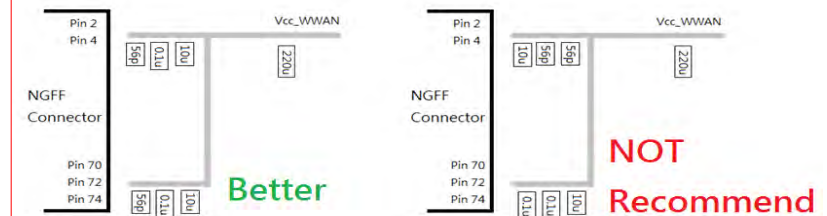
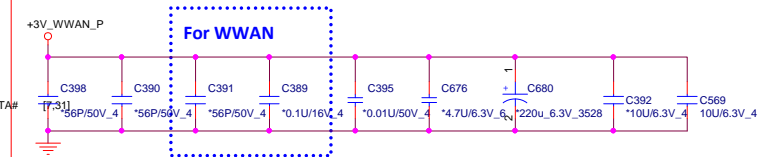
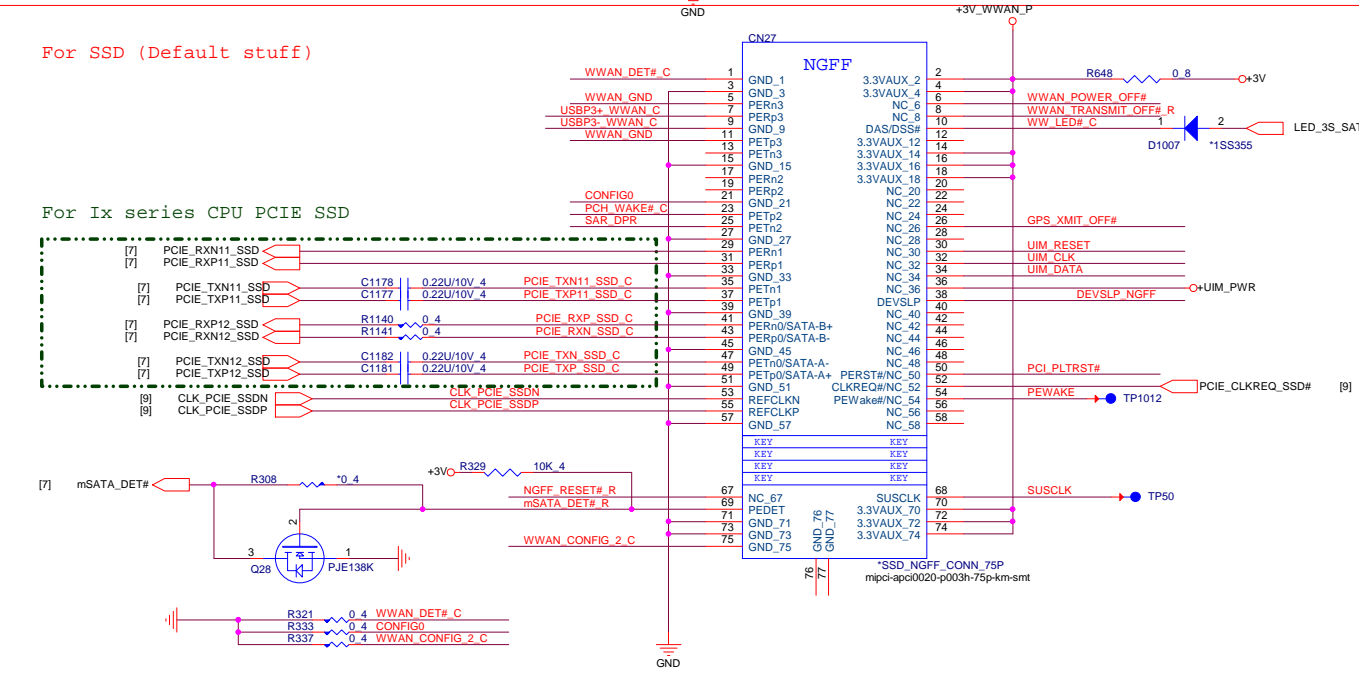
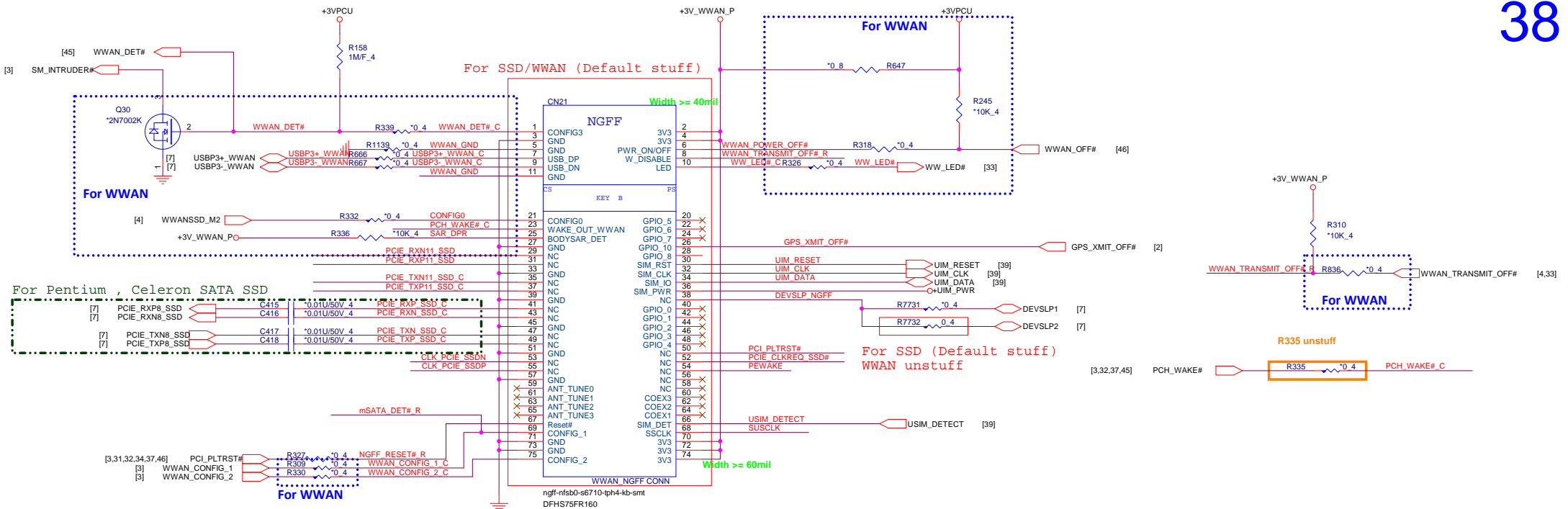


NB5

PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 36 -- TS and Accelerometer	Rev 1A
Date: Thursday, May 12, 2016		Sheet 36 of 65





	+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0	ON	High	High	High
S3	ON	High	Low	Low
S4	ON	Low	Low	Low
S5	ON	Low	Low	Low

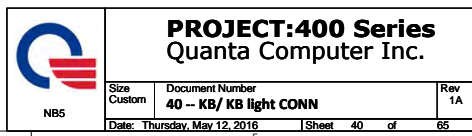


Trace Length and Routing

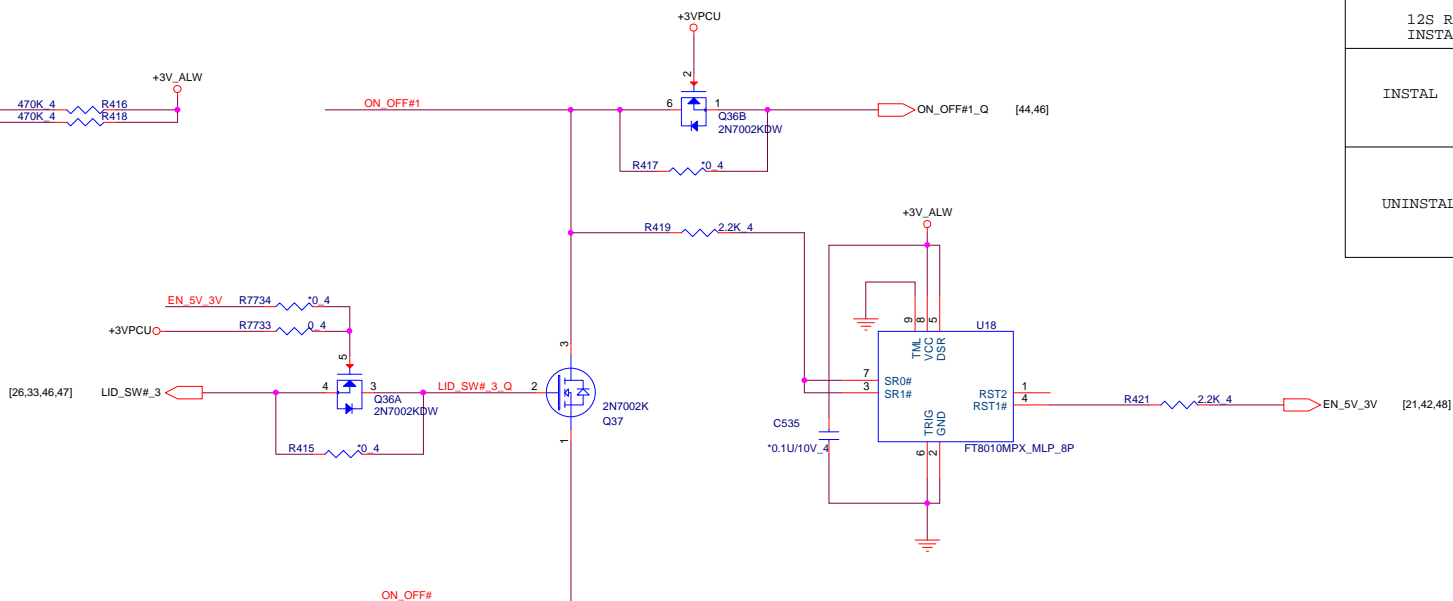
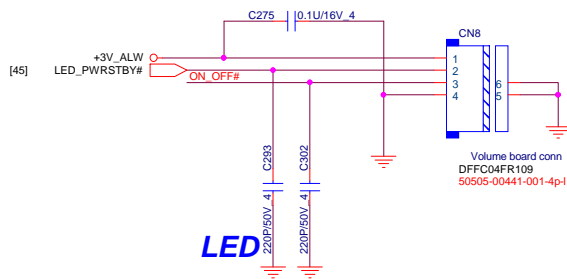
- ←

SIM Power↵

WWW.AliSaler.Com




Power Botton Connector



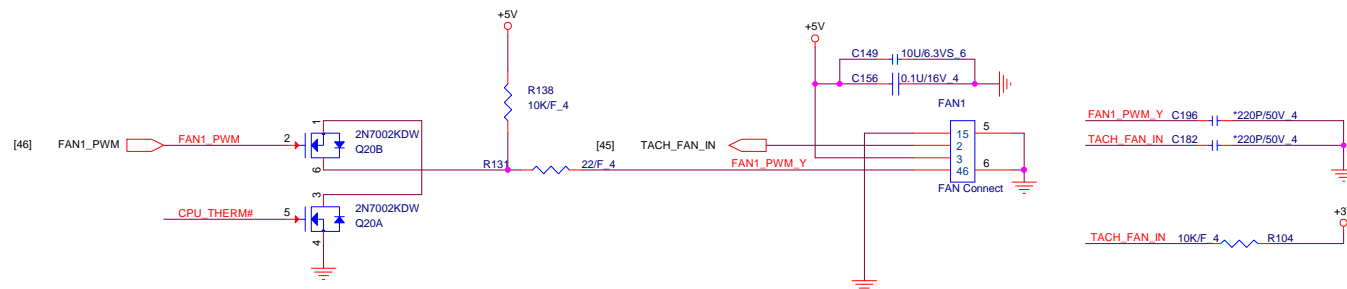
12S RESET MODE INSTAL FOR DB0		
INSTAL	R10702 R10704 R10701 U9068	R10703 R581 R595
UNINSTAL	R10754 Q7080	R10755 Q7081

[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63] +3V
[8,27,29,30,40,42,43,54,58,63] +5V
[9,48,51,52,58,62,63] +3V_ALW



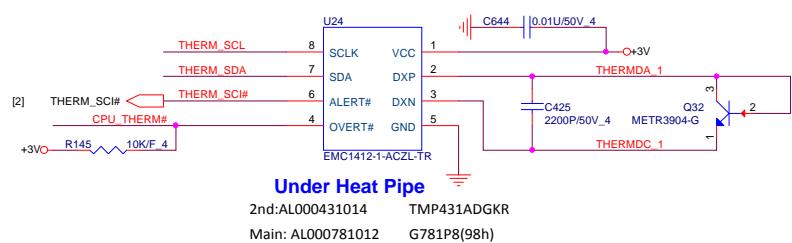
PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 41 -- Power Button/ HW Reset	Rev 1A
Date: Thursday, May 12, 2016	Sheet 41 of 65	



Thermal sensor

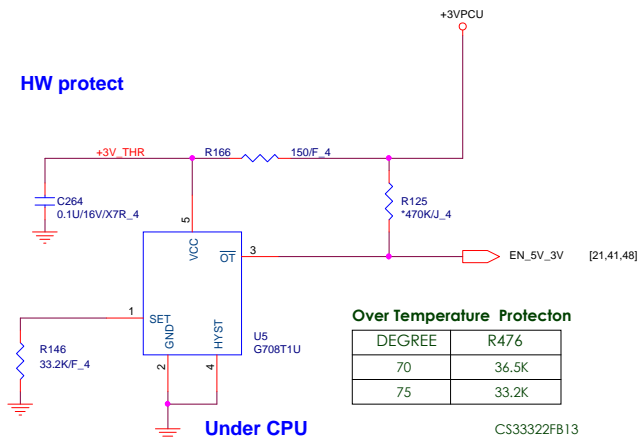
CPU Thermal Sensor



Under Heat Pipe

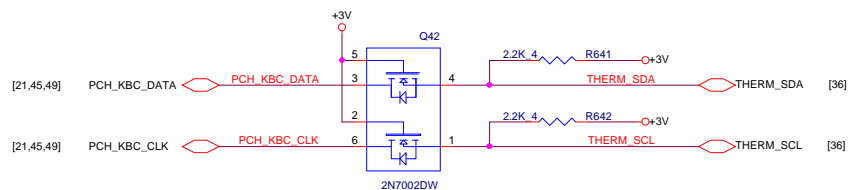
2nd: AL000431014 TMP431ADGKR
Main: AL000781012 G781P8(98h)

HW protect




Under CPU

$$RSET \text{ (K OHM)} = 0.0012T^2 - 0.9308T + 96.147$$

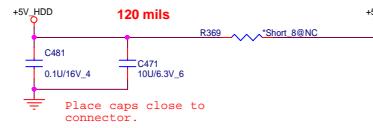
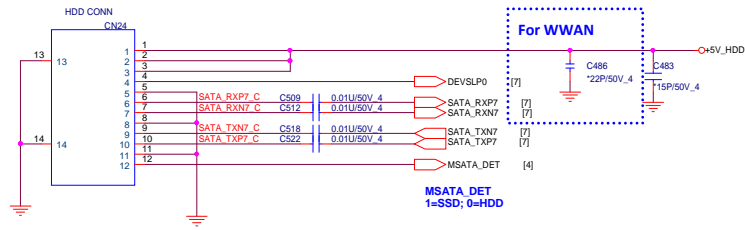


[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,44,45,47,51,56,58,59,63]
[9,41,48,51,52,58,62,63]

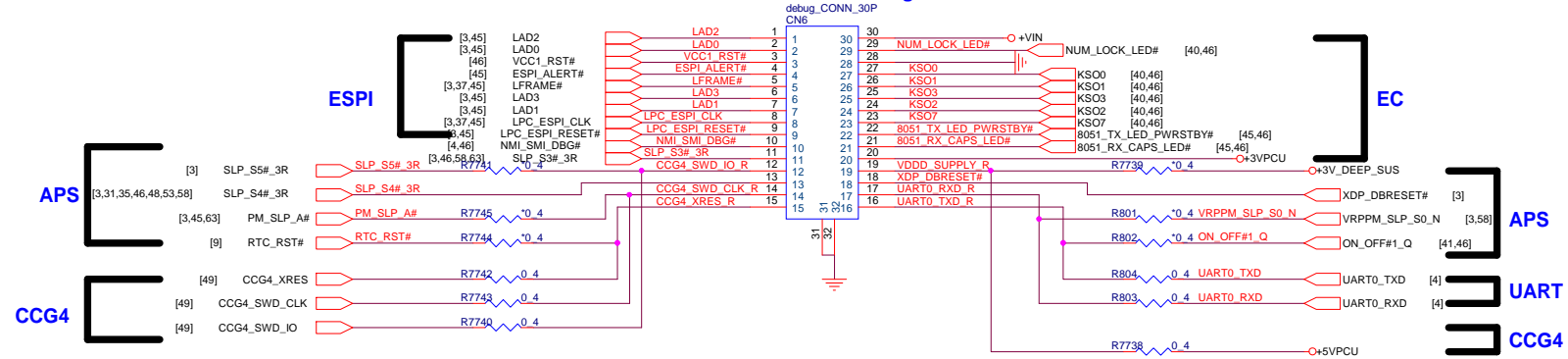
+3V
+3V_ALW

 NB5	PROJECT:400 Series Quanta Computer Inc.	
	Size Custom	Document Number 42-- FAN and Thermal IC
	Date: Thursday, May 19, 2016	Sheet 42 of 65

SATA-HDD



ESPI+EC+APS debug conn on MB



LPC_ESPI_CLK *0.4 R154 *10P/50V_4 C240

UART0_RXD R39 49.9K/F 4
UART0_TXD R43 49.9K/F 4


+3V R538 10K 4 XDP_DBRESET#

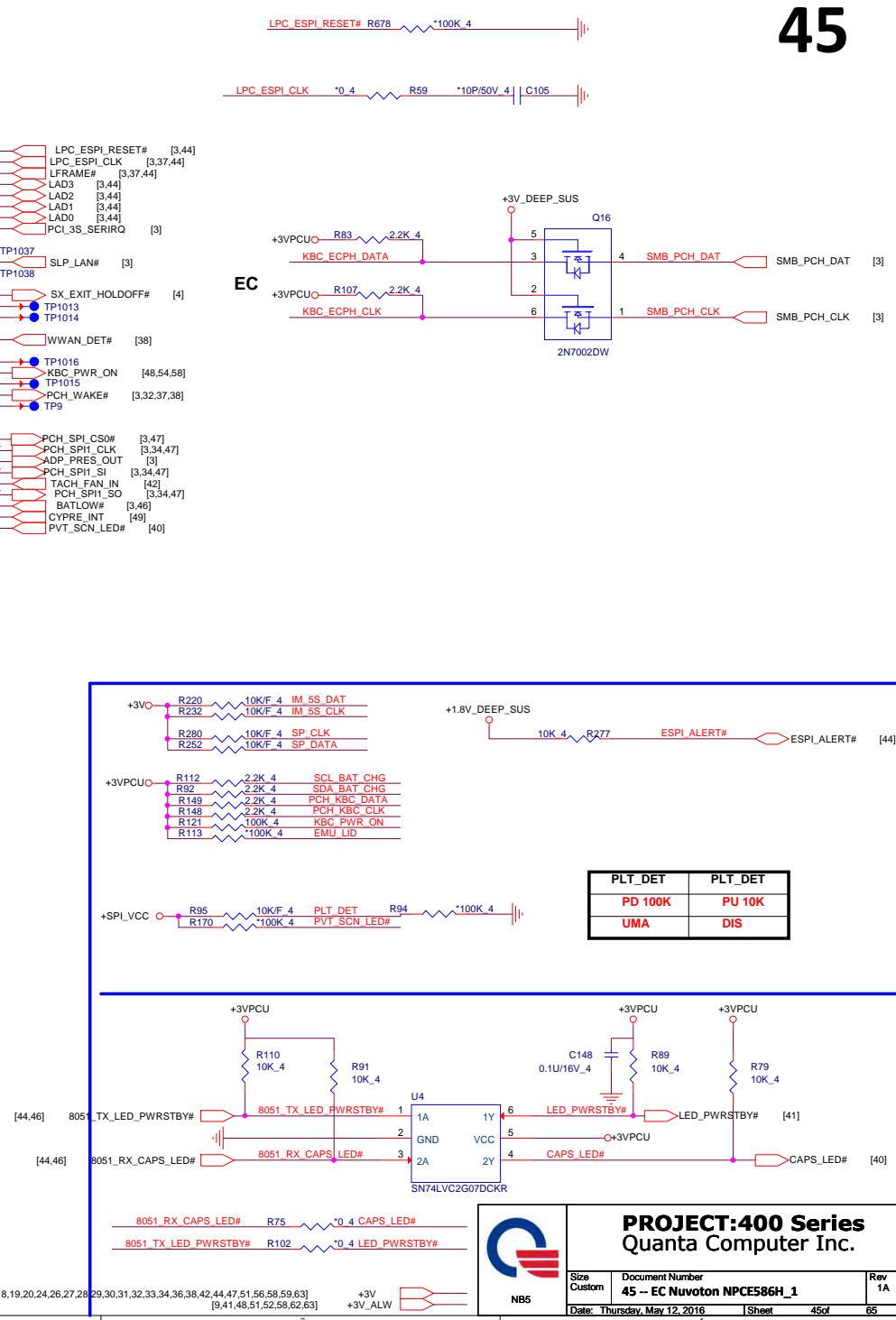
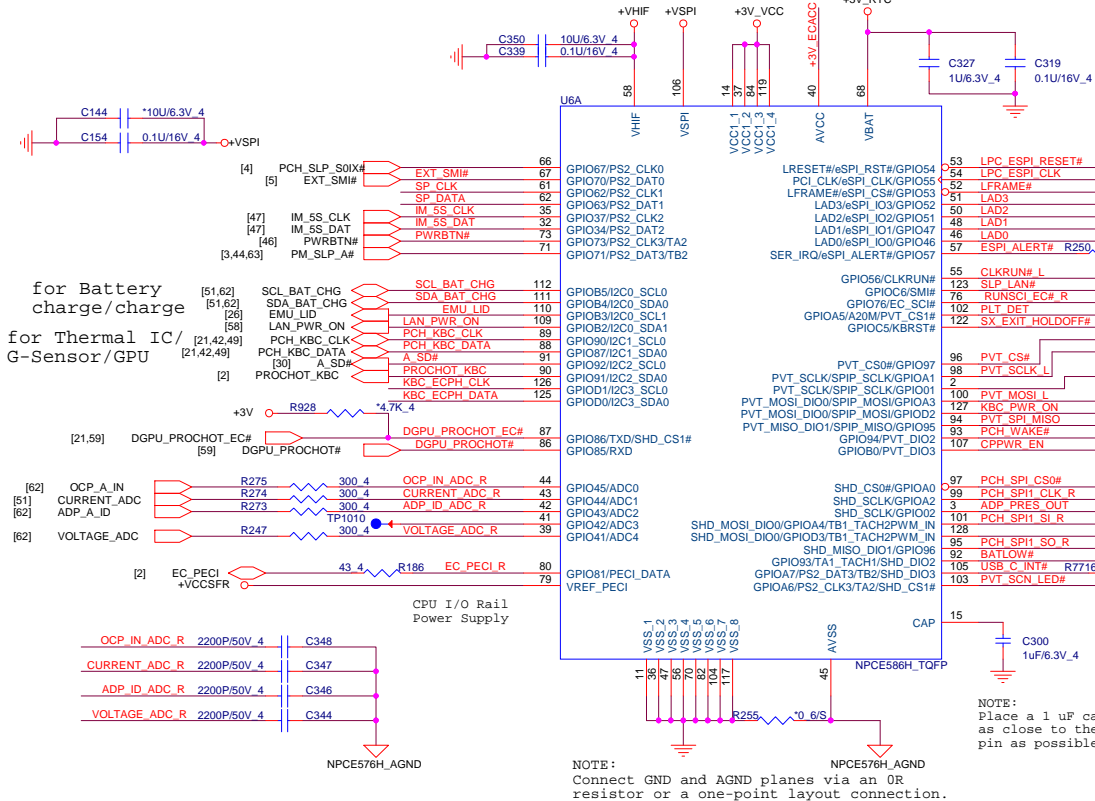
LPC & ESPI TABLE

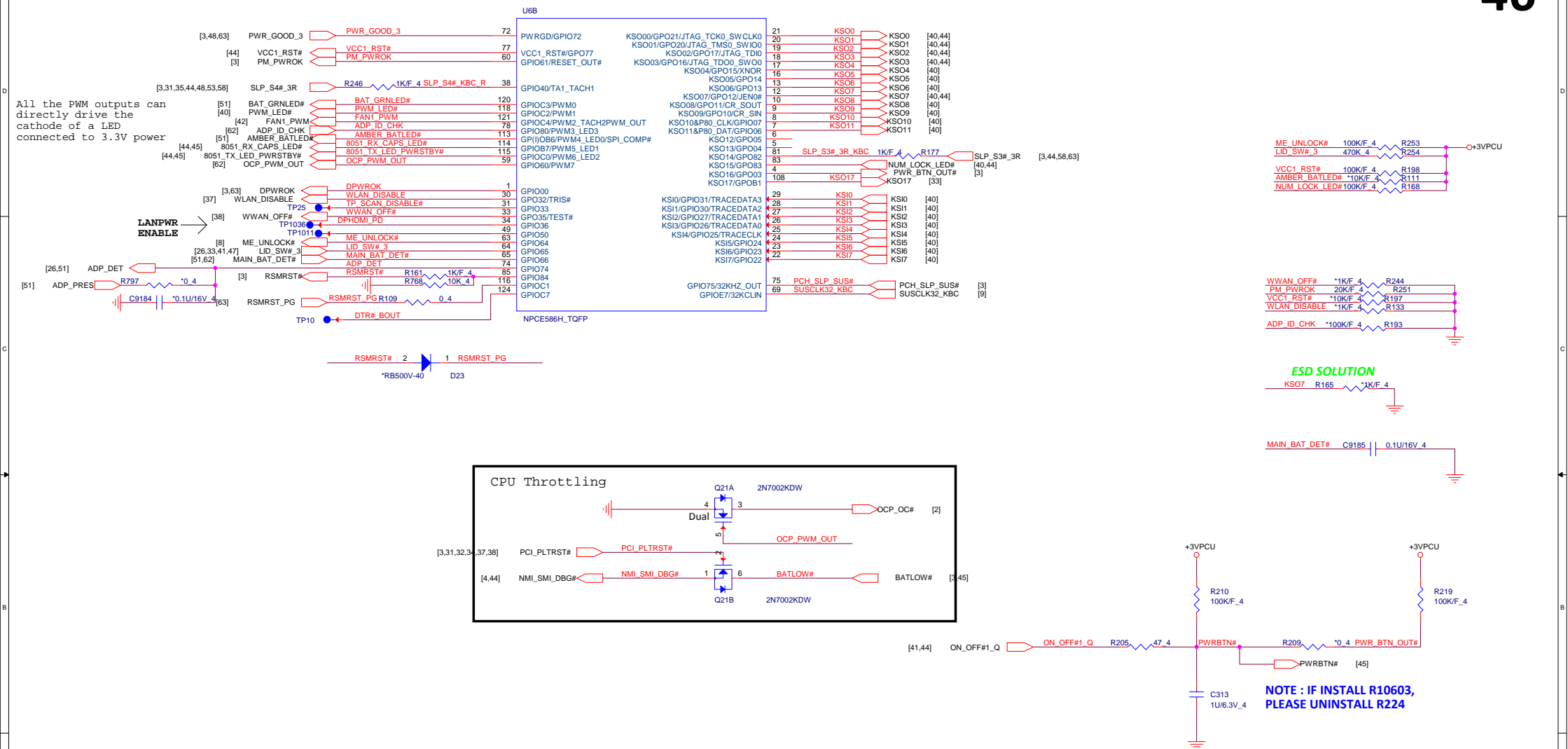
	LPC MODE	ESPI MODE
R771	INSTAL	UNINSTAL
R769	UNINSTAL	INSTAL
R770	INSTAL	UNINSTAL

LPC & ESPI TABLE

	LPC MODE	ESPI MODE
R658	Ra INSTAL	UNINSTAL
R646	Rb INSTAL	UNINSTAL
R659	Rc INSTAL	UNINSTAL
R656	Rd INSTAL	UNINSTAL
R649	Re INSTAL	UNINSTAL
R657	Rf INSTAL	UNINSTAL
R249	Rg INSTAL	UNINSTAL
R147	Rh INSTAL	UNINSTAL
R120	Ri INSTAL	UNINSTAL
R276	Rj INSTAL	UNINSTAL
R678	Rk UNINSTAL	INSTAL

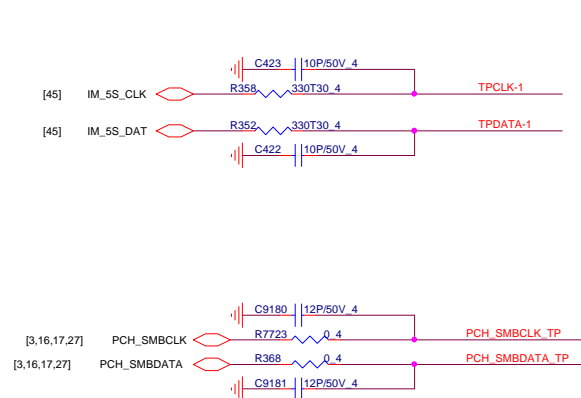
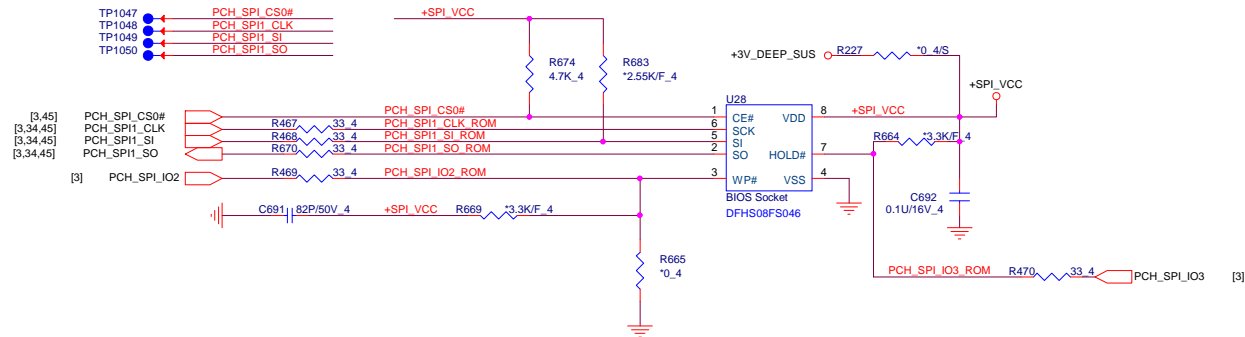
 NB5	PROJECT:400 Series		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number 44 -- EC & eSPI/UART debug conn	
Date: Thursday, May 12, 2016		Sheet 44 of 65	





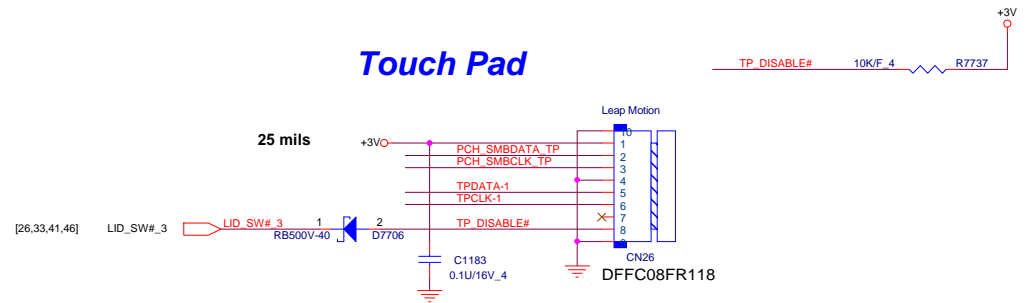
Vender	Size	P/N
GD	128MB	AKE2DF0KQ00
Winbond	128MB	AKE3DZKNK00
Socket		DFHS08FS046


PCH SPI ROM(CLG)

PCH 6*5mm WSON 16M
SPI ROM Socket

CLICK PAD
Address: 0x20(7 bit)

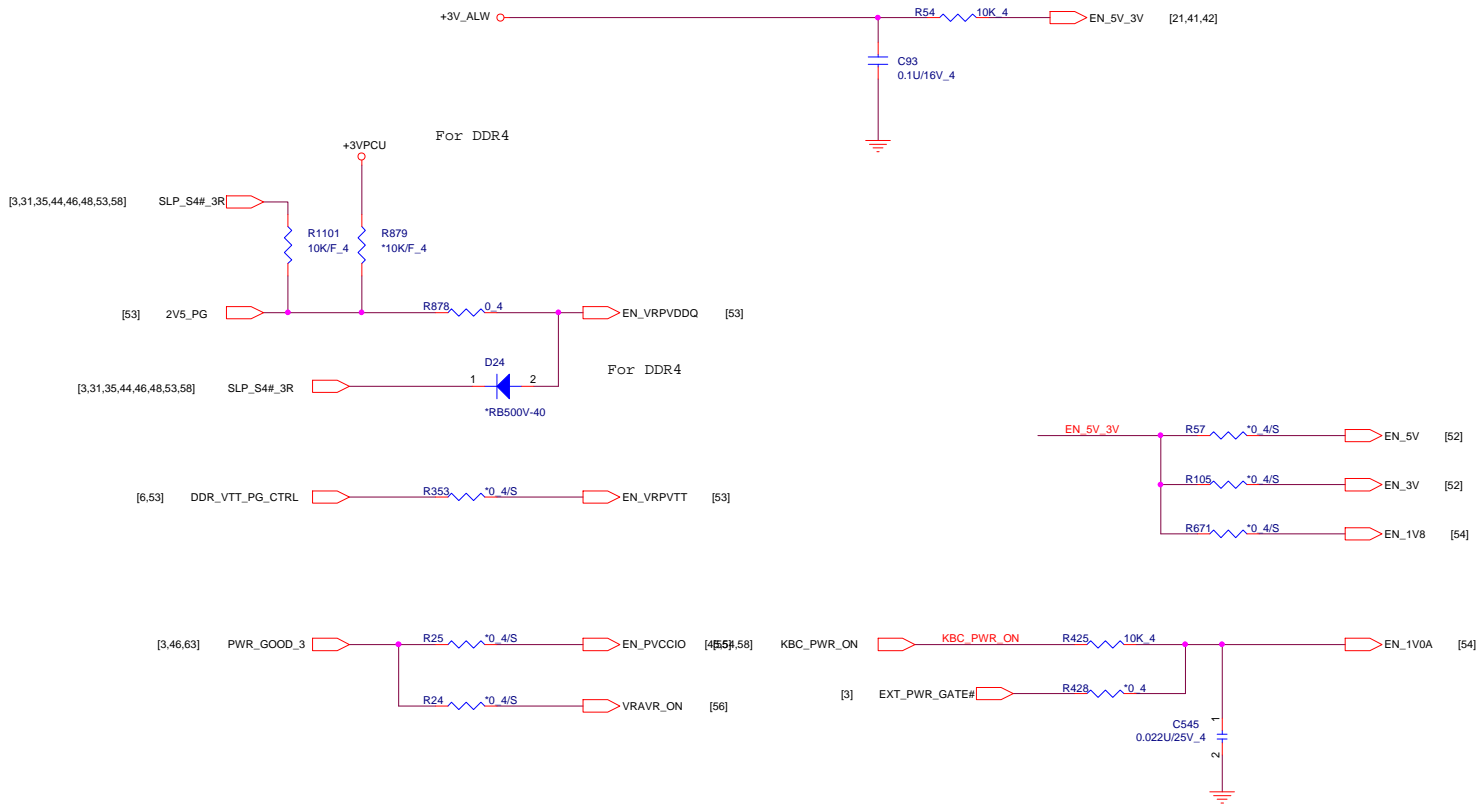
Touch Pad



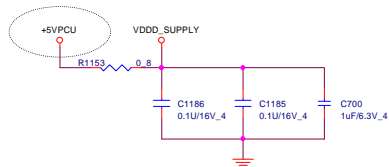
	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 47 - Flash(KBC+PCH)	Rev 1A
	Date: Thursday, May 12, 2016	Sheet 47 of 65	

400 series 1001

POWER TO EE NET NAME CONNECTION

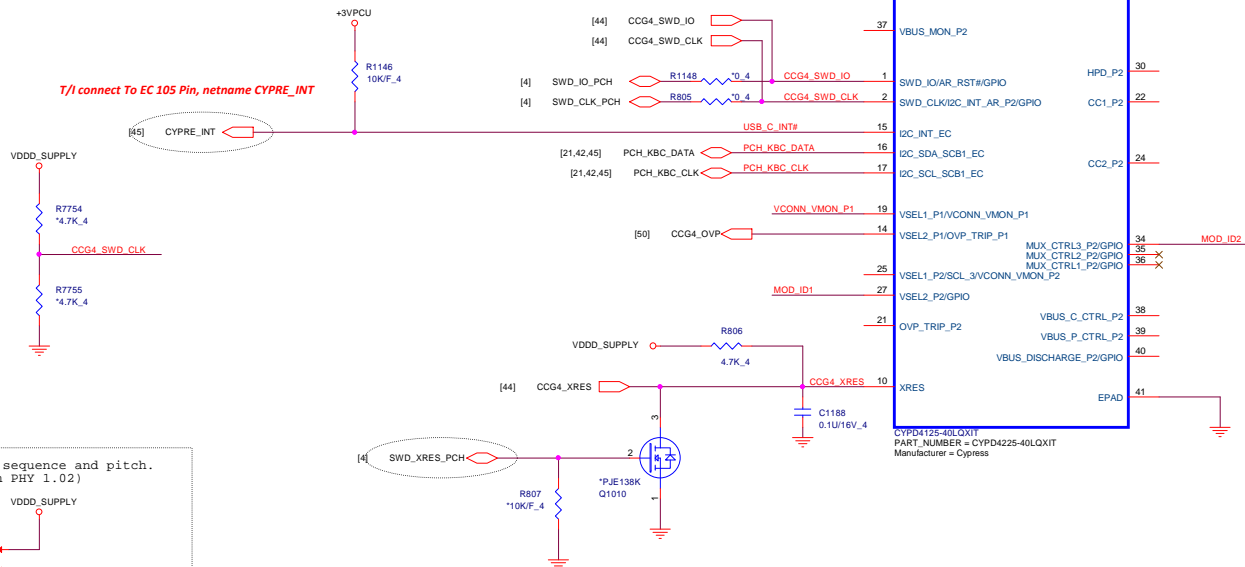


SI, 2/22, Change 5V

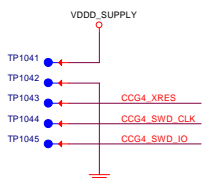


Note:
The above resistor divider network is needed only when VDDO_SUPPLY is 3.3V.
Don't place R58 and R60 resistors when VDDO_SUPPLY is 5V.
Use 0ohm resistors for R57 and R59 when VDDO_SUPPLY is 5V.

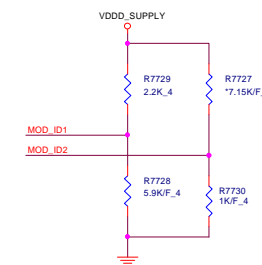
T/I connect To EC 105 Pin, netname CYPRE_INT



test points sequence and pitch.
(2.54mm with PHY 1.02)



MOD_ID	Pull high	Pull down
L0	None	1K
L1	7.1K	1K
L5	3.09K	5.1K
L6	2.2K	5.9K



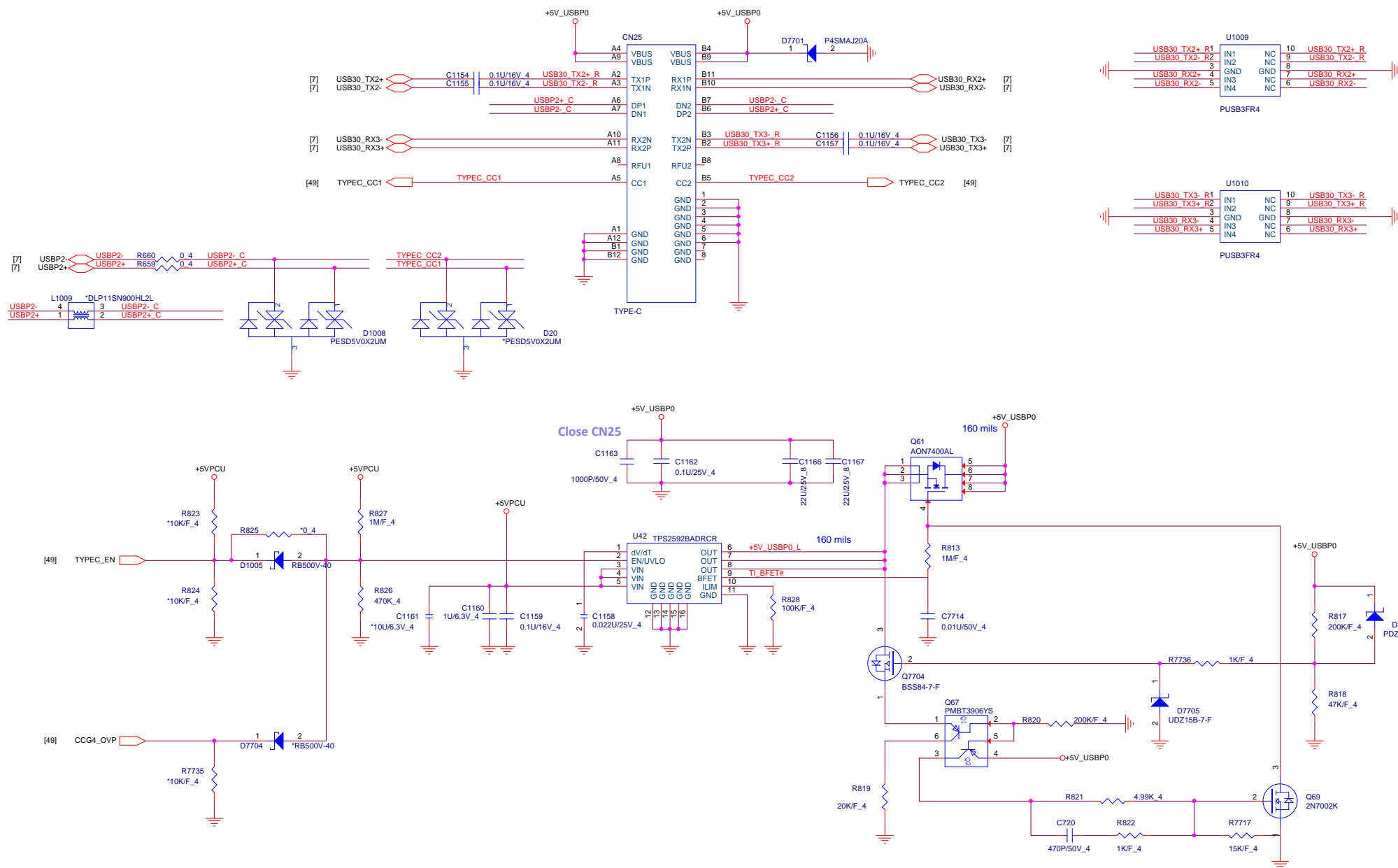
MOD_ID1 and MOD_ID2 pins connect to ABC in CCG4.

	Platform ID		Dual Port	Single Port		
	MOD_ID1	MOD_ID2	Description (Dual port)	Dual Port CFGID	Description (Single)	Single Port CFGID
Non TBT Slice Modules	L7	L0	Discrete GFX module for Slice	CFG0		
	L7	L1	HDD module for Slice	CFG1		
	L7	L2	ODD module for Slice	CFG1		
	L7	L3	Legacy I/O module for Slice	CFG1		
	L7	L4			Communication	CFG0
	L7	L5	Future use			
	L7	L6	Future use			
TBT platforms	L7	L7	Future use			
	L0	x	TBT Module for Slice	CFG2		
	L1	x			Slice Gen2	CFG1
Non TBT Desktop Platforms	L2	x			800 & 600, AIO Addon Card	CFG2
	L5	L0	Slice Gen1 & Gen2	CFG3	Slice Gen1	CFG3
	L5	L1	800 & 600 Series	CFG4	800 & 600, 400 Series (DPF)	CFG4
Non TBT Notebook Platforms	L5	L2	Future		800 & 600 (DPF+DP)	CFG5
	L6	L6	DRP+DP on two ports	CFG5	DPF only	CFG4
	L6	L1			DRP+DP on single port	CFG5



PROJECT:400 Series
Quanta Computer Inc.

Size Document Number
49 -- Cypress CCG1
Date: Friday, May 20, 2016 Sheet 49 of 65

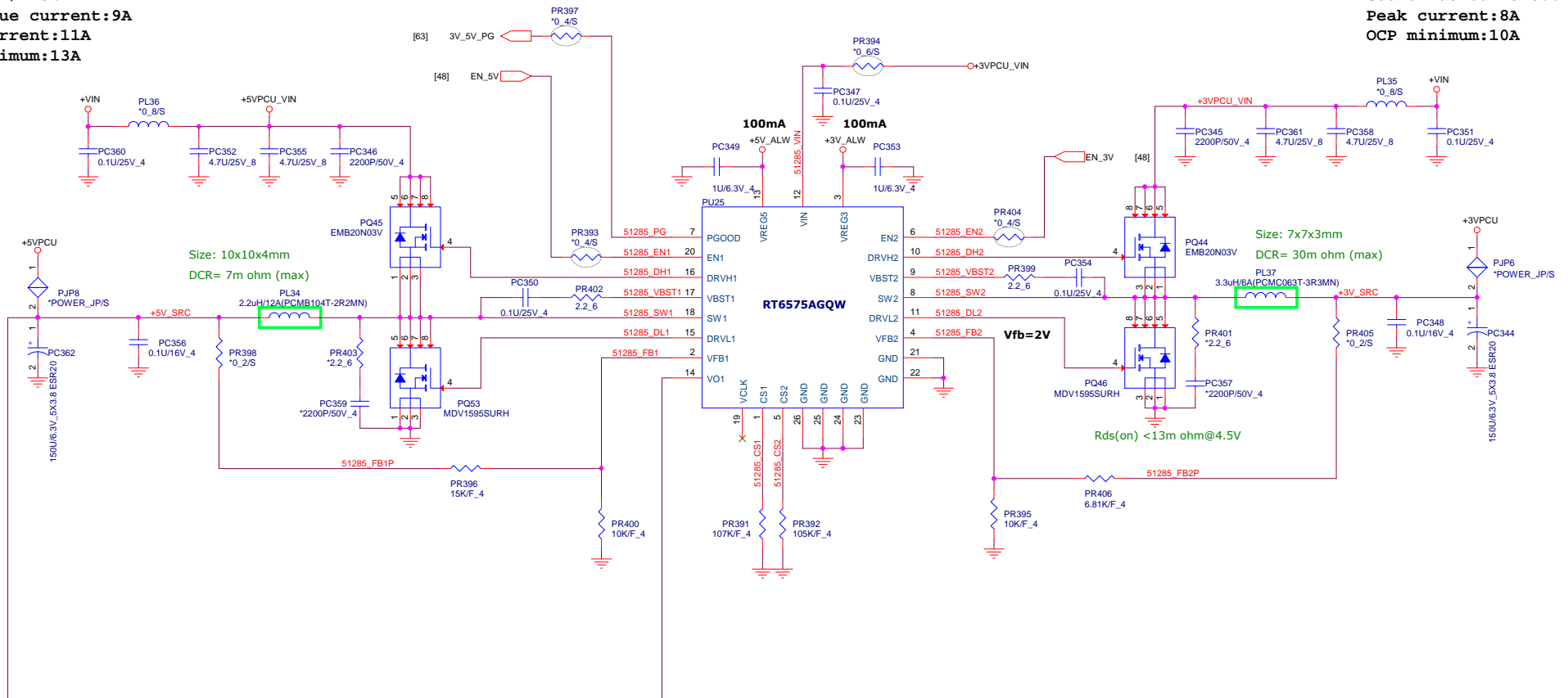





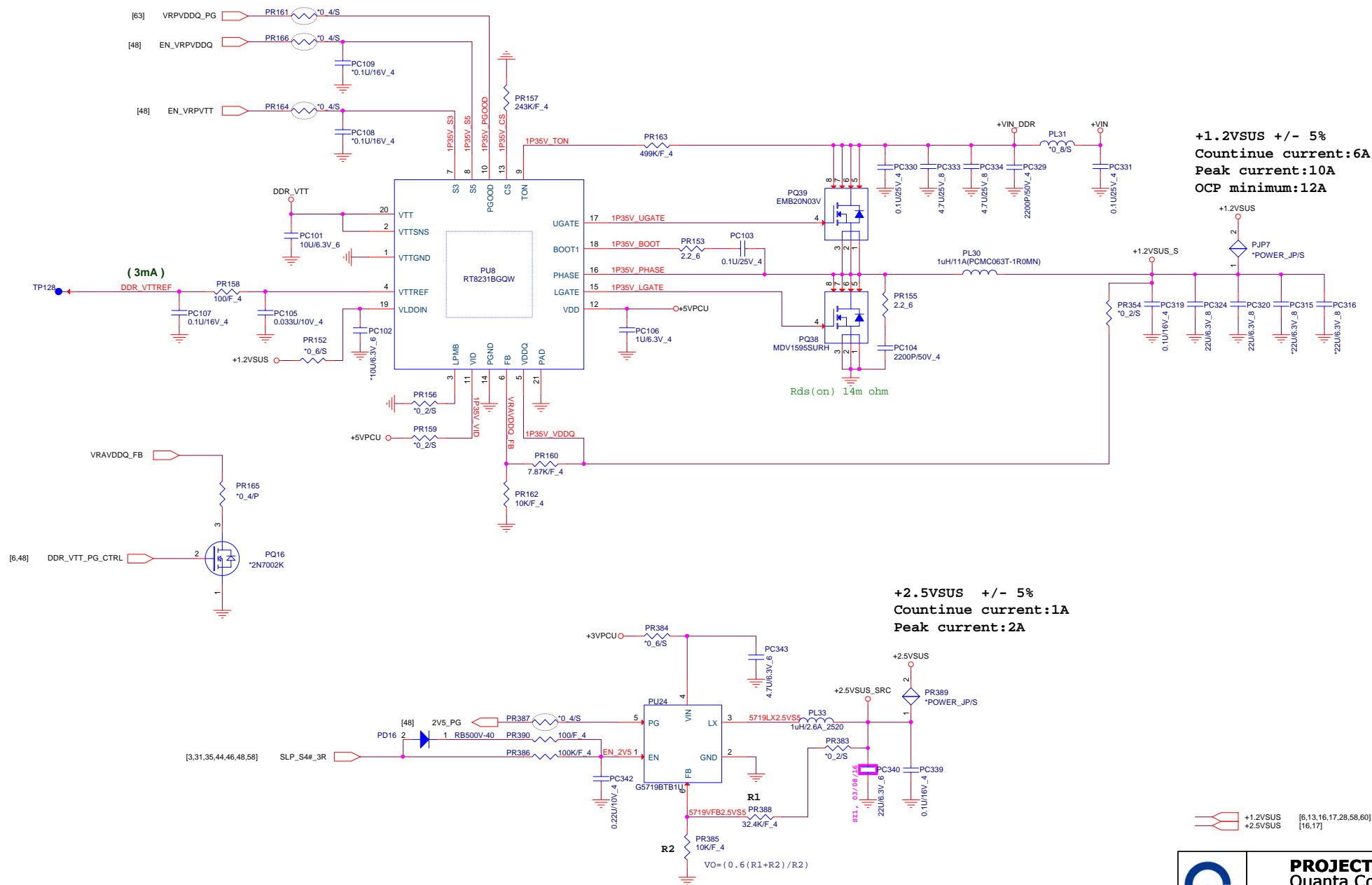
+3VPCU [3,10,33,37,38,40,41,42,44,45,46,48,49,51,53,55,58,60,62,63]
+5VPCU [28,31,35,44,49,50,51,53,54,56,57,58,59,60,61,63]

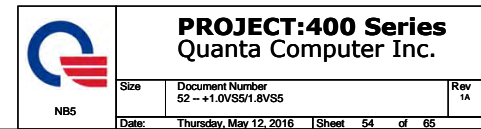
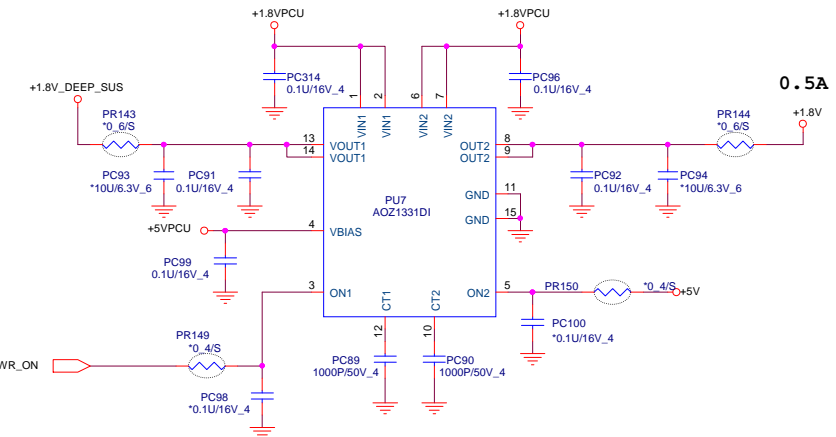
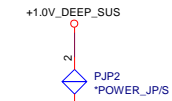
+5VPCU +/- 5%
Continue current:9A
Peak current:11A
OCP minimum:13A

+3VPCU +/- 5%
Continue current:6A
Peak current:8A
OCP minimum:10A



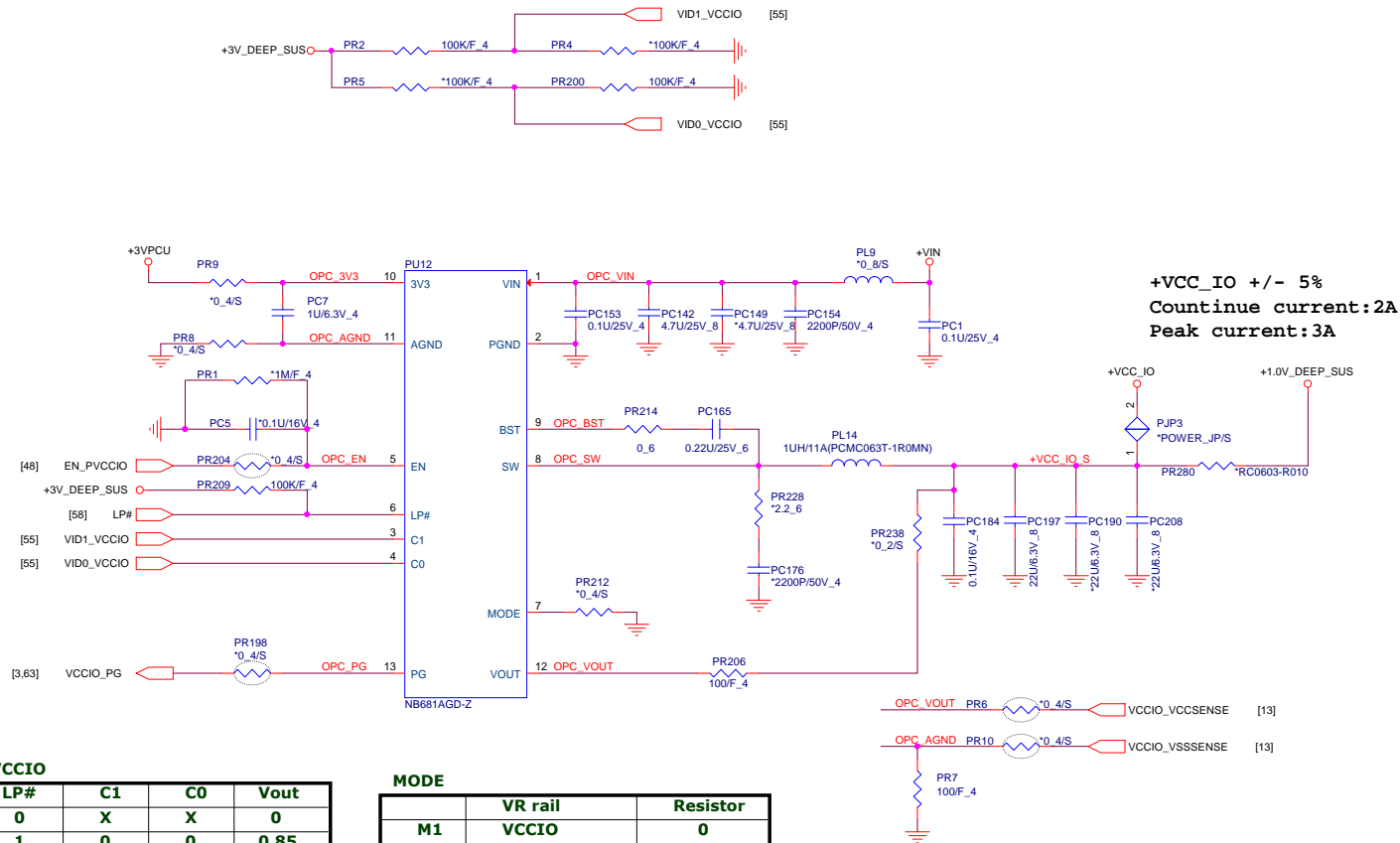
 PROJECT:400 Series Quanta Computer Inc.		
Size	Document Number 50 - 3/5VS5 (SY8208B/SY8208C)	Rev 1A
Date:	Thursday, May 12, 2016	Sheet 52 of 65

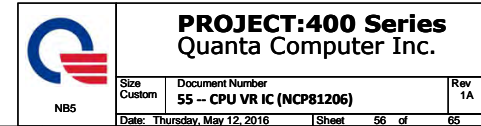


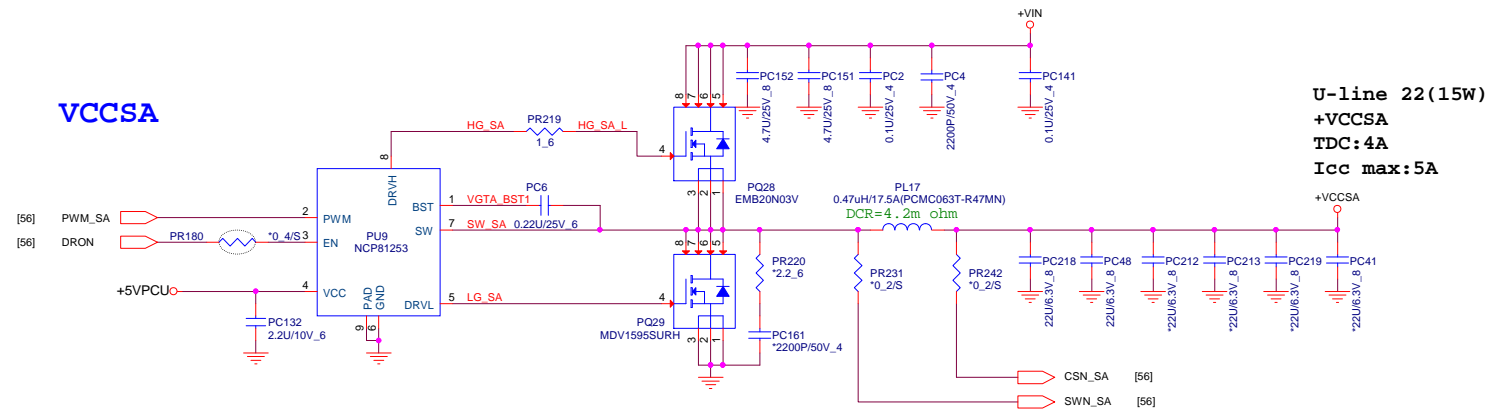


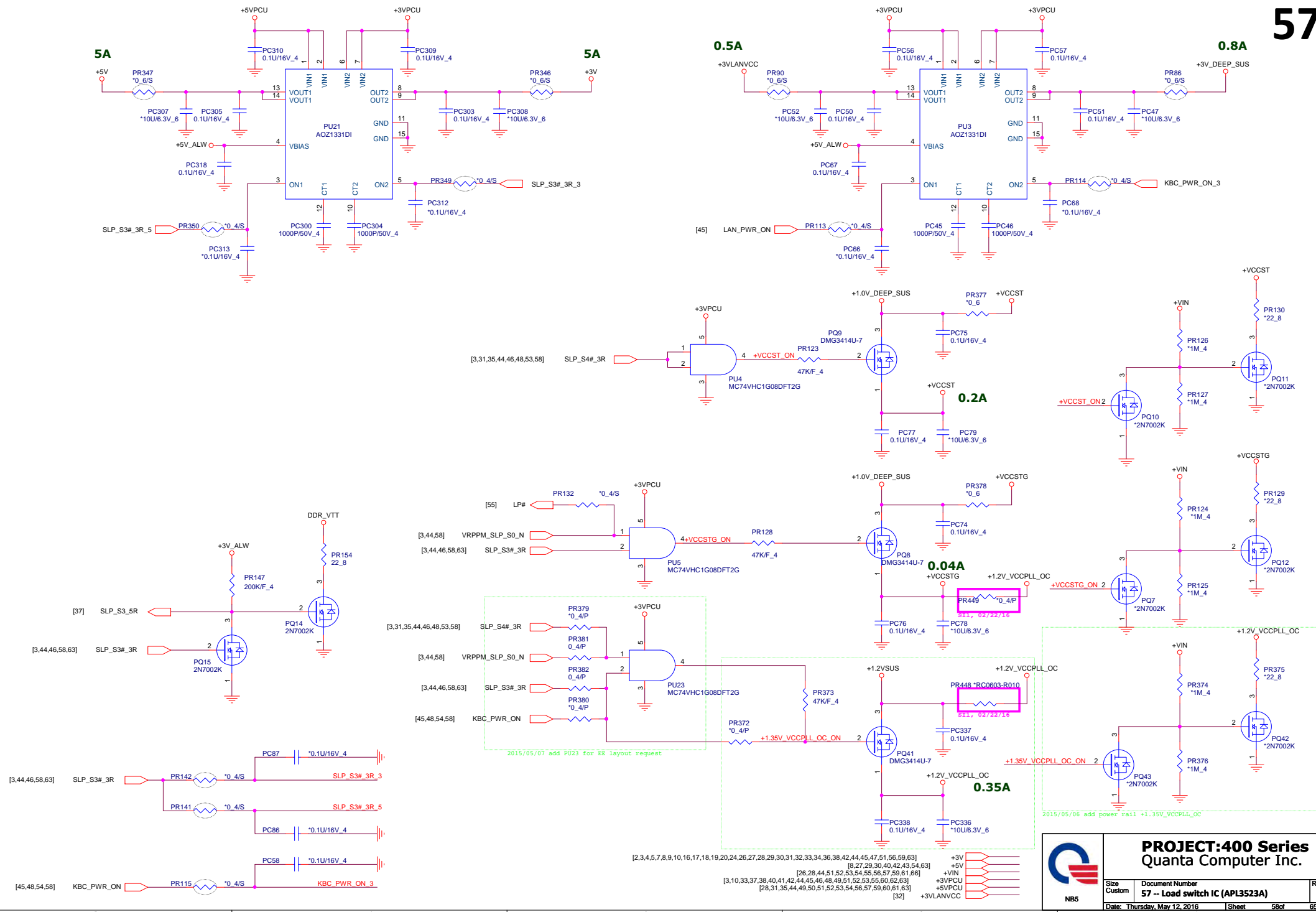
[26,28,44,51,52,53,54,56,57,58,59,61,66]
[9,41,48,51,52,58,62,63]
[5,13]

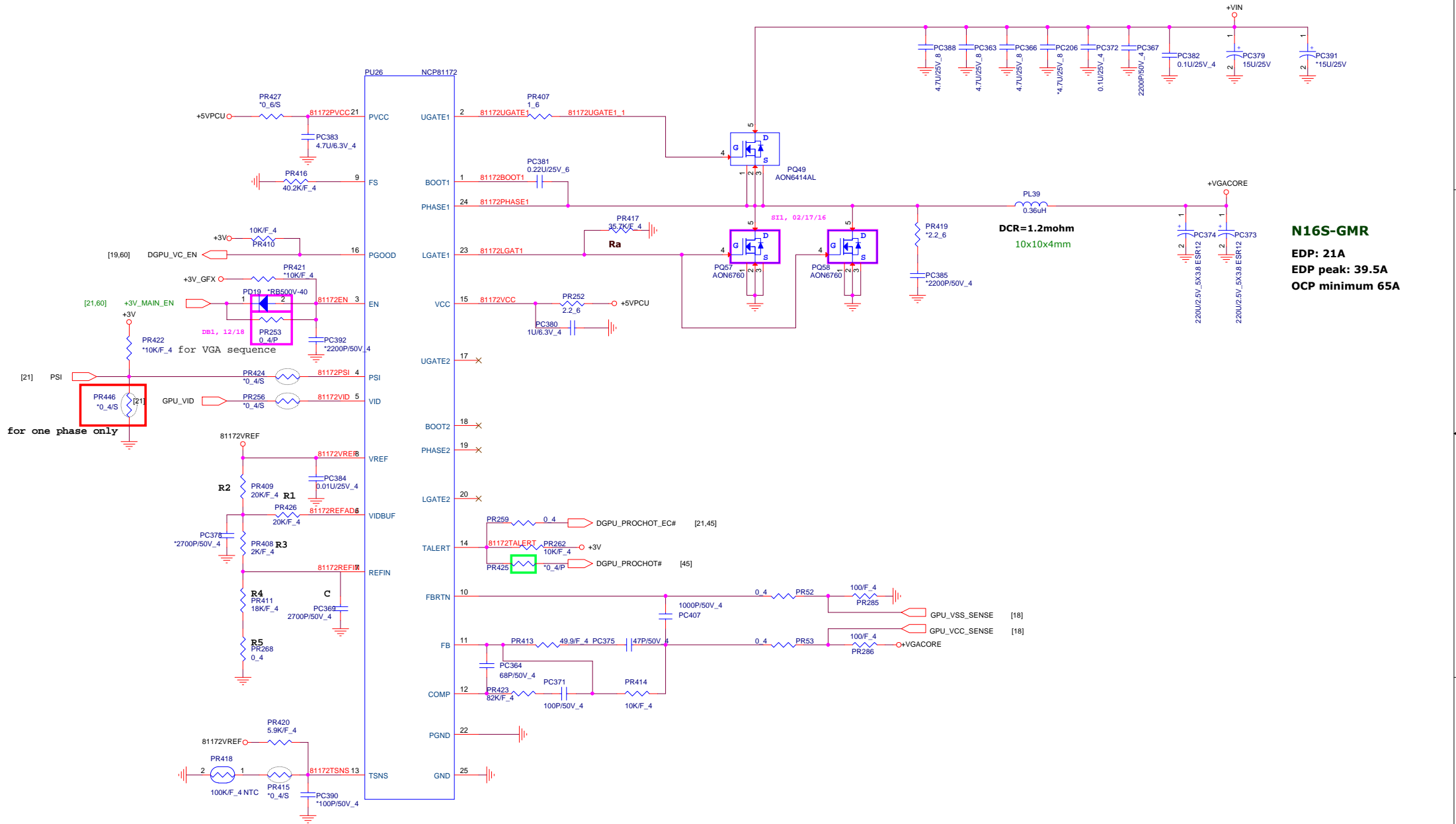
+VIN
+3V_ALW
+VCC_IO

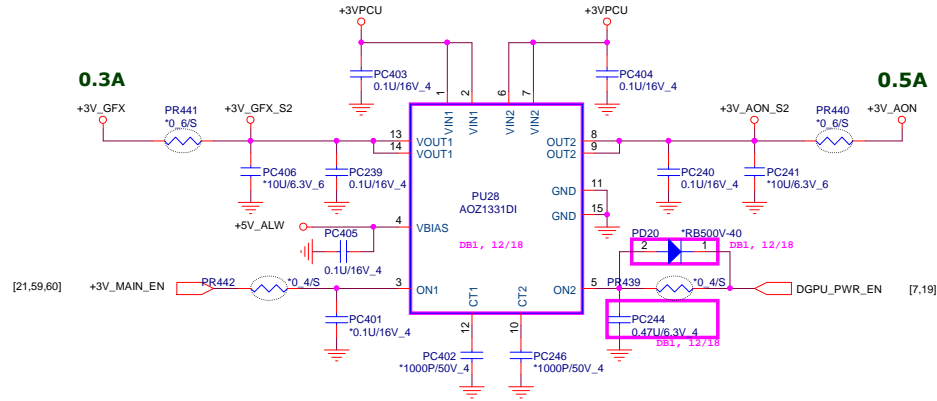
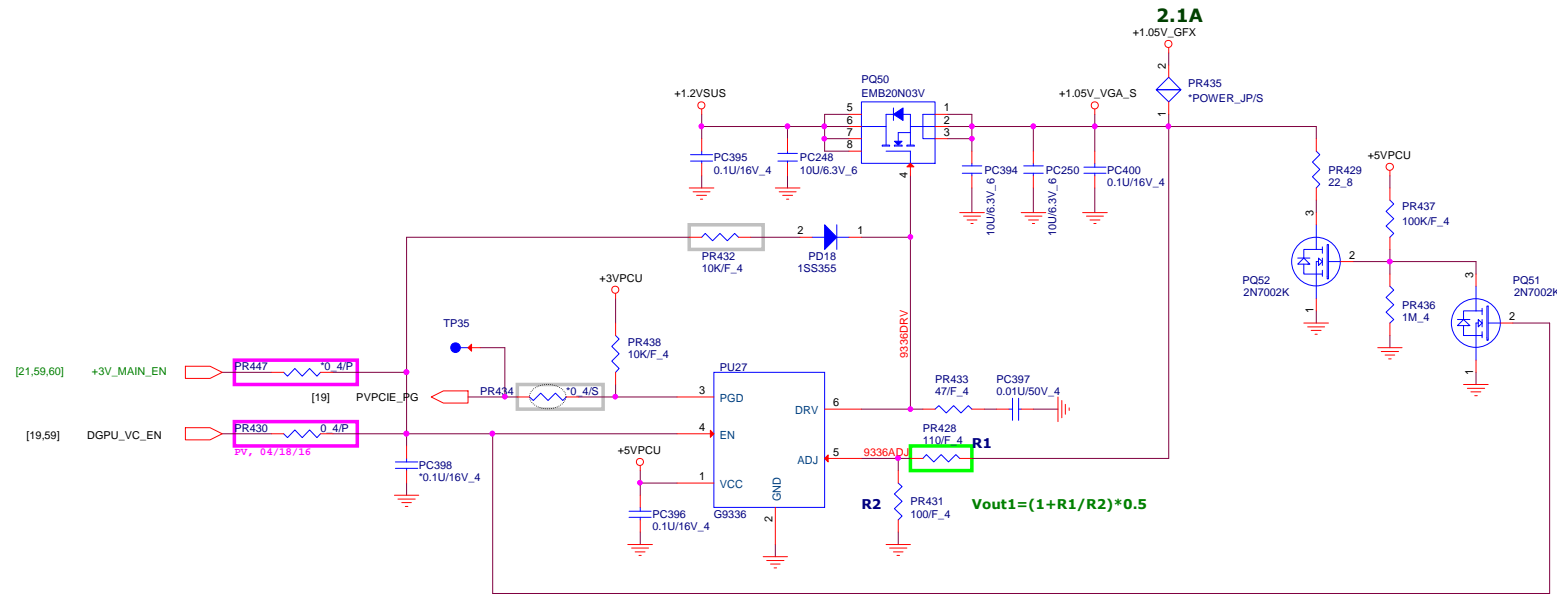


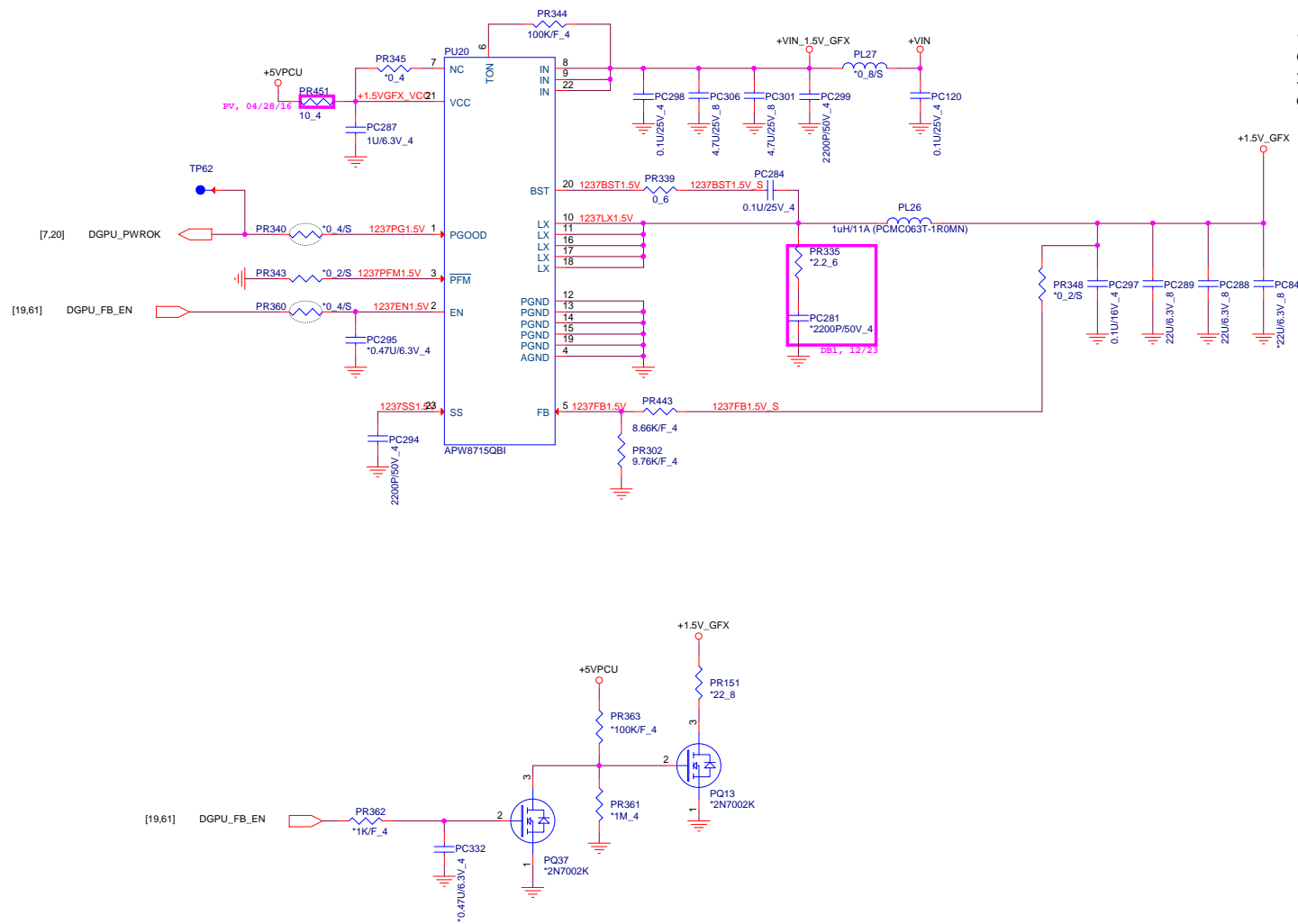




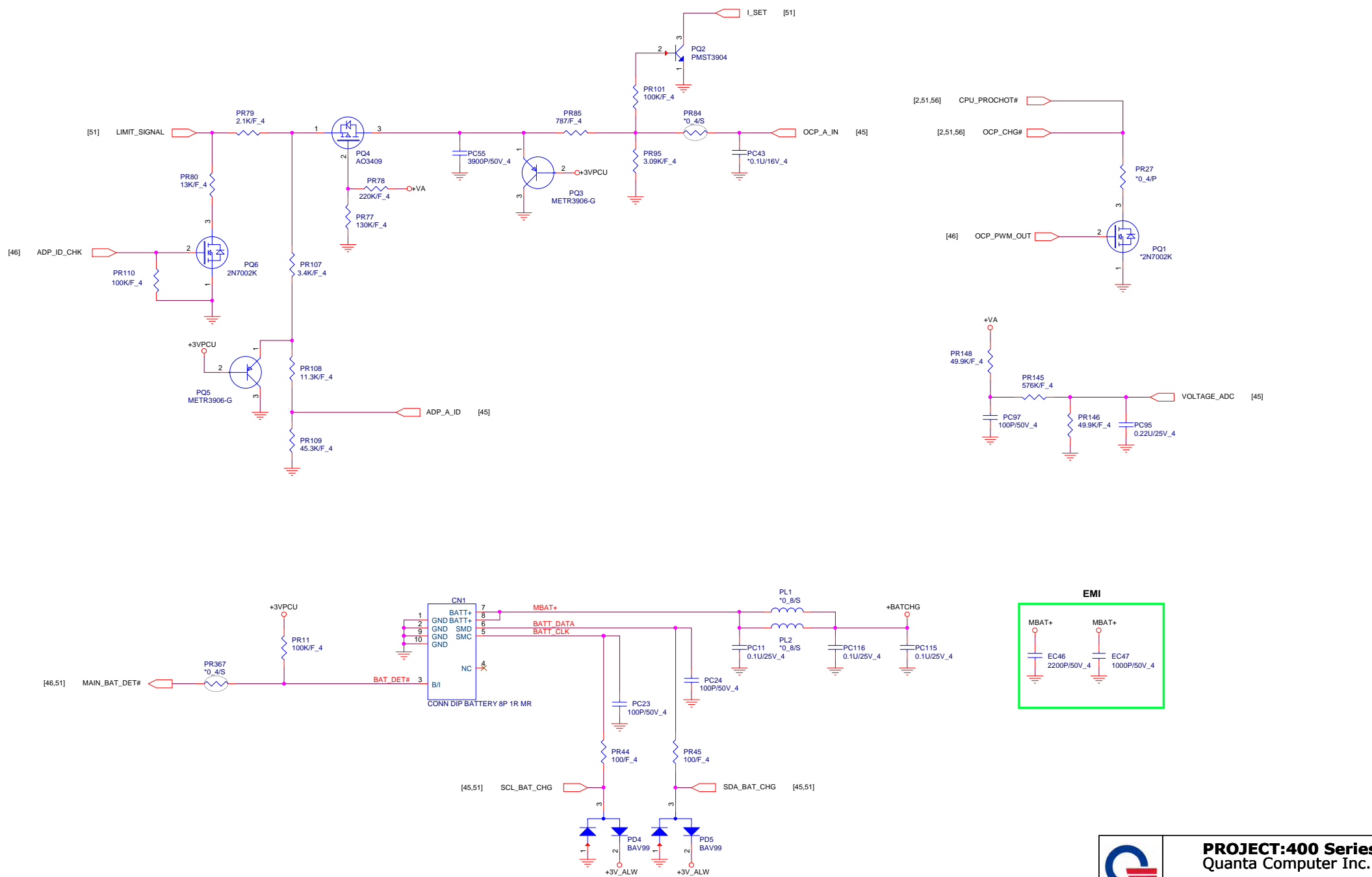









Adapter OCP



**PROJECT:400 Series**
Quanta Computer Inc.

Size	Document Number	Rev
	62 - CHARGER II	1A
Date:	Thursday, May 12, 2016	Sheet 62 of 65

POK CKT

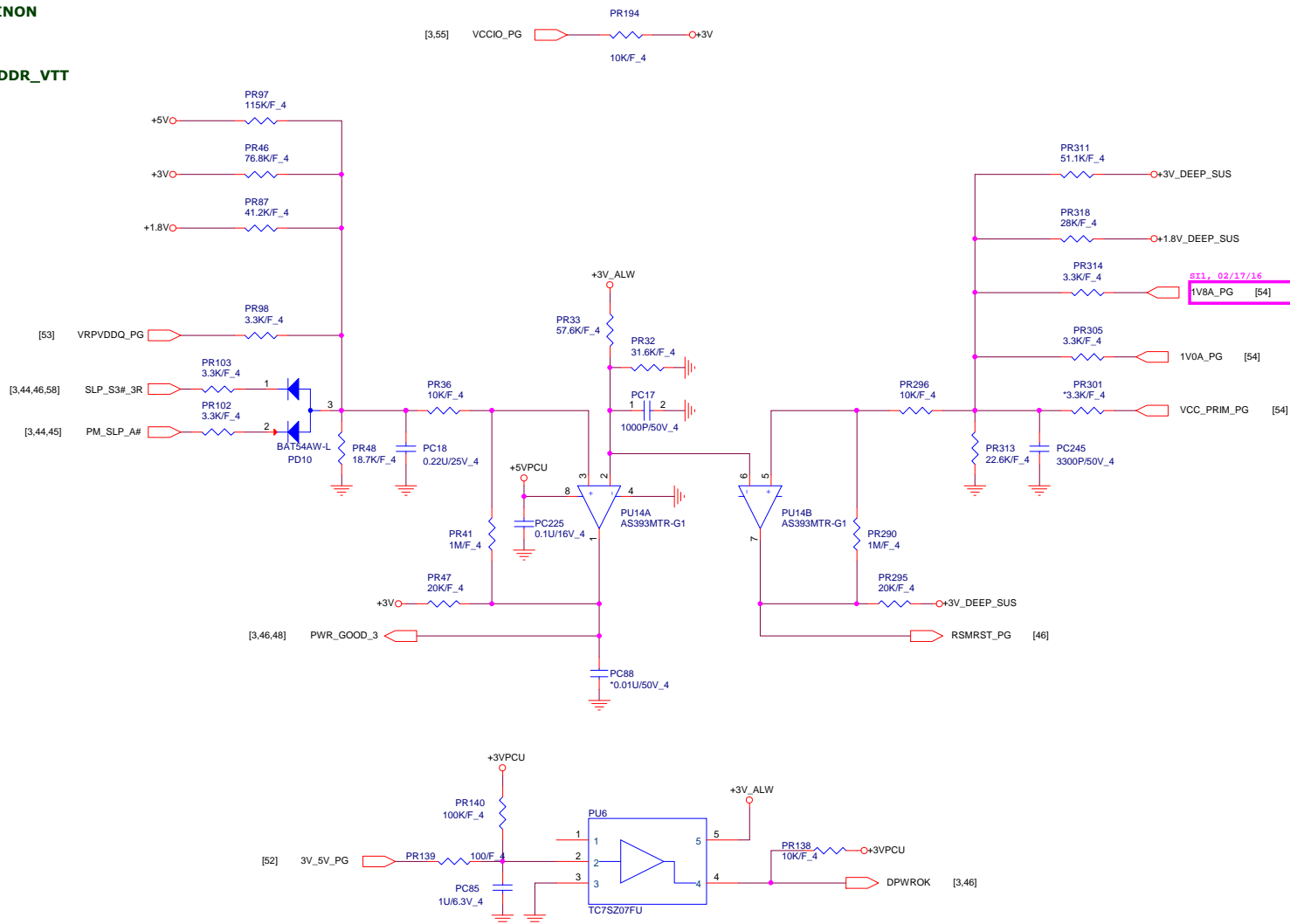
PM_SLP_S4# = SUSON

PM_SLP_S3# = MAINON

+V5S = +5V

+V3S = +3V

+V0.75S = +0.75V_DDR_VTT



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59]

[8,27,29,30,40,42,43,54,58]

[9,41,48,51,52,58,62]

+3V

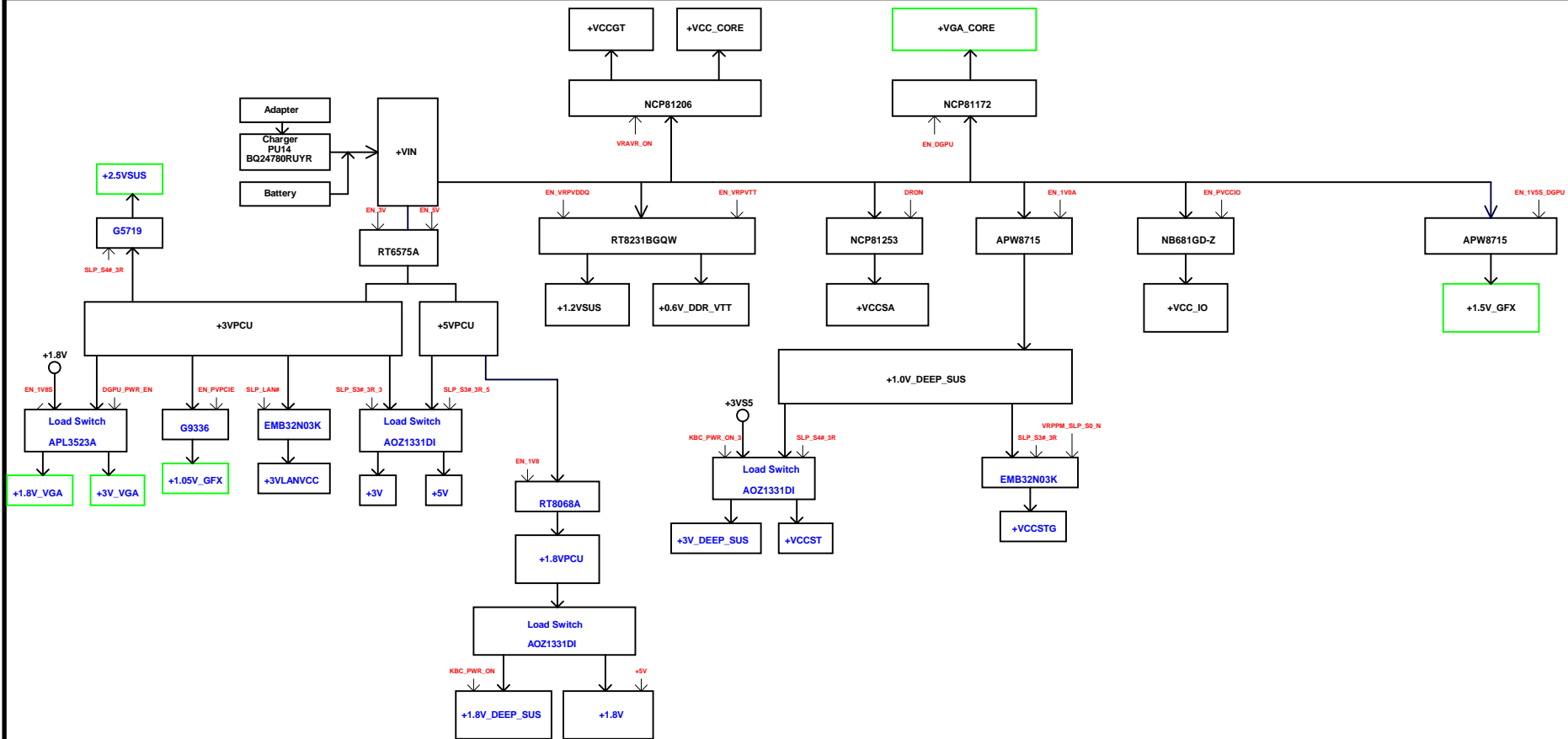
+5V

+3V_ALW

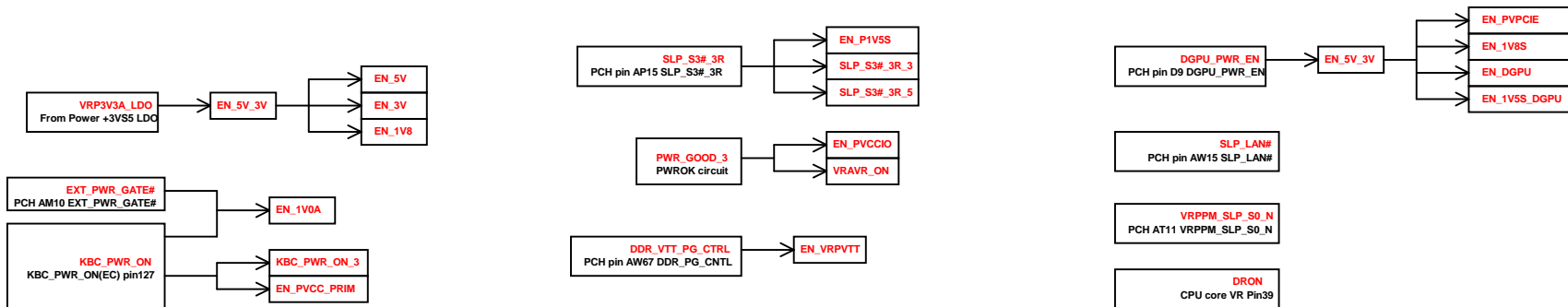


PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	63 - PWROK	1A
Date: Thursday, May 12, 2016	Sheet 63 of 65	

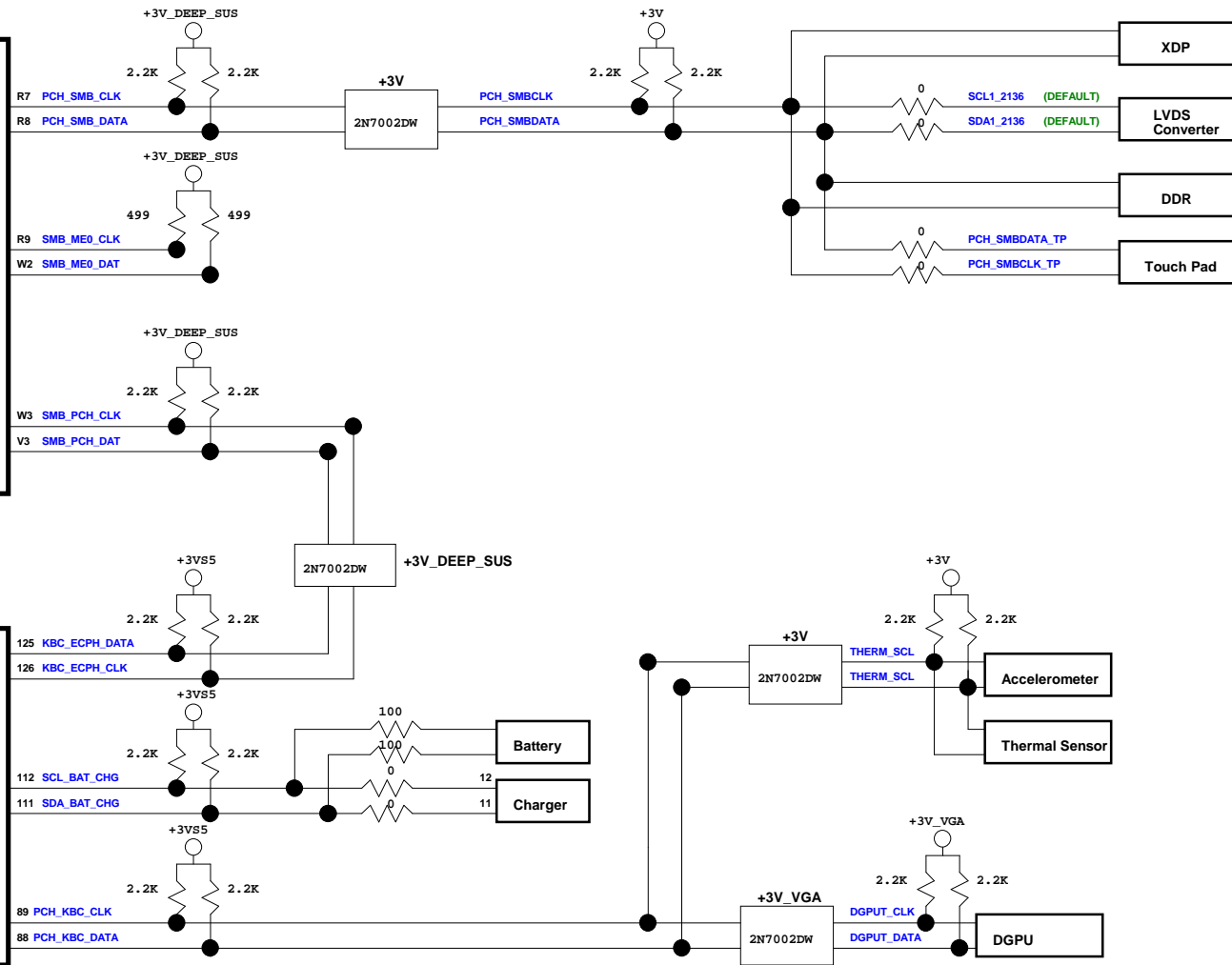


POWER ENABLE PIN



SKYLAKE U

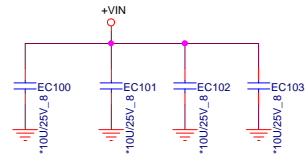
EC
NPCE586H




Example: *499/F_4 and *0_6/S
 * means none-installed
 499 means value
 F means 1%
 _4 means 0402 size
 /S means short pad

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC



 NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 66 -- EMI and ISN	Rev 1A
	Date: Thursday, May 12, 2016	Sheet 66 of	66